SDRAM Operation

Last updated 2/8/24

SDRAM - Operation

- SDRAM Topology - Micron 512Mb SDRAM

  - From a Micron SDRAM spec:

  SDRAMs offer substantial advances in DRAM operating performance, including the ability to synchronously burst data at a high data rate with automatic column-address generation, the ability to interleave between internal banks to hide precharge time, and the capability to randomly change column addresses on each clock cycle during a burst access.

SDRAM - Operation

- SDRAM Topology - Micron 512Mb SDRAM
  - The 512Mb SDRAM is a high-speed CMOS, dynamic random-access memory containing 536,870,912 bits.
  - It is internally configured as a quad-bank DRAM
  - It has a synchronous interface (all signals are registered on the positive edge of the clock signal, CLK).
  - Each of the x4's 134,217,728-bit banks is organized as 8192 rows by 4096 columns by 4 bits.
  - Each of the x8's 134,217,728-bit banks is organized as 8192 rows by 2048 columns by 8 bits.
  - Each of the x16's 134,217,728-bit banks is organized as 8192 rows by 1024 columns by 16 bits.

SDRAM - Operation

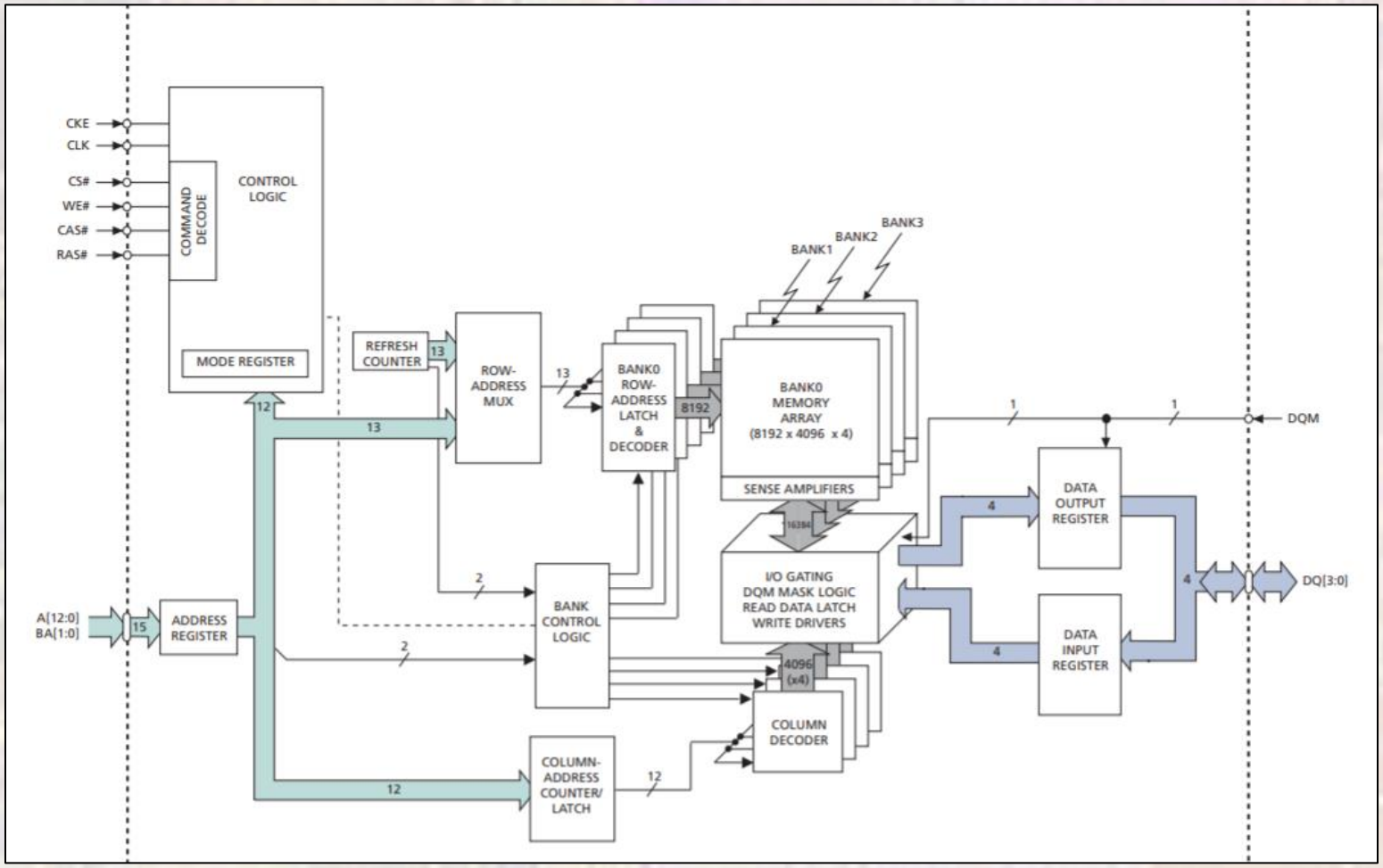
- SDRAM Topology - Micron 512Mb SDRAM
  - Read and write accesses to the SDRAM are burst-oriented
    - Accesses start at a selected location and continue for a programmed number of locations in a programmed sequence.
    - Accesses begin with the registration of an ACTIVE command, which is then followed by a READ or WRITE command.
    - The address bits registered coincident with the ACTIVE command are used to select the bank and row to be accessed (BA[1:0] select the bank; A[12:0] select the row).
    - The address bits registered coincident with the READ or WRITE command are used to select the starting column location for the burst access.
    - The SDRAM provides for programmable read or write burst lengths (BL) of 1, 2, 4, or 8 locations, or the full page, with a burst terminate option.

SDRAM - Operation

- SDRAM Topology - Micron 512Mb SDRAM
  - The SDRAM uses an internal pipelined architecture to achieve high-speed operation.
  - This architecture is compatible with the 2n rule of prefetch architectures
  - It also allows the column address to be changed on every clock cycle to achieve a highspeed, fully random access.
  - Precharge Capability
    - An auto precharge function may be enabled to provide a self-timed row precharge that is initiated at the end of the burst sequence.
    - Precharging one bank while accessing one of the other three banks will hide the PRECHARGE cycles and provide seamless, high-speed, random-access operation.

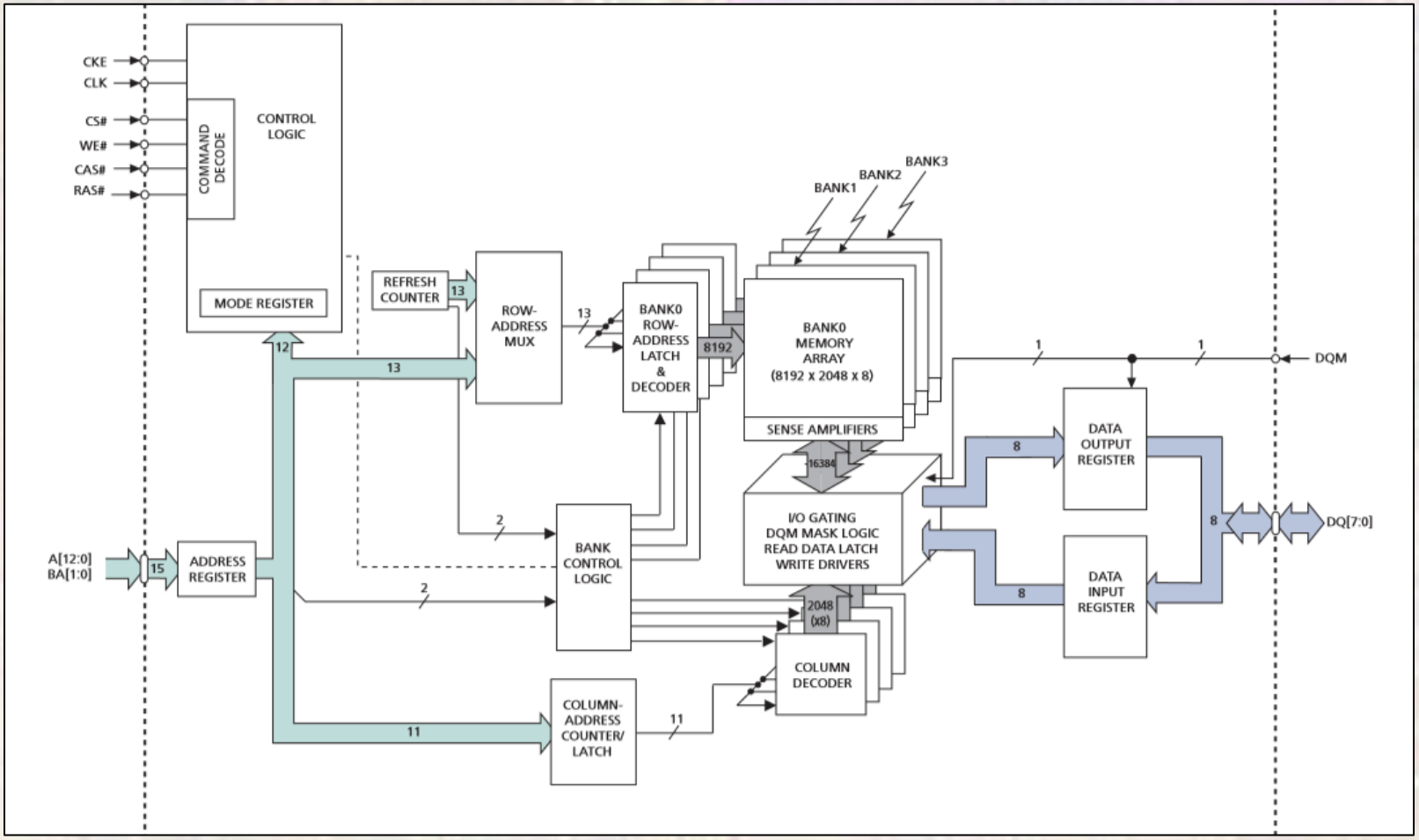
SDRAM - Operation

- SDRAM
  - 512Mb : 128Mx4



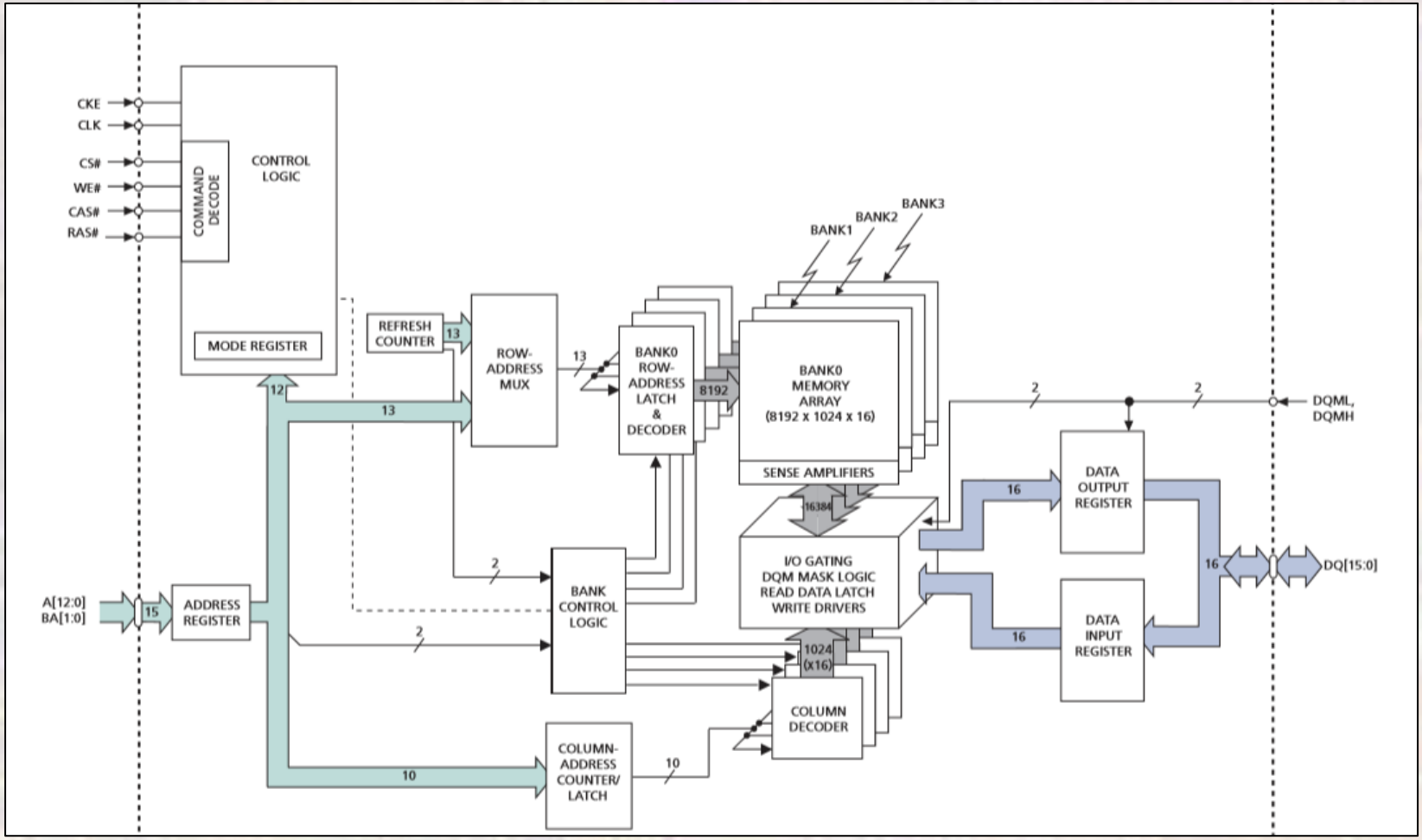
SDRAM - Operation

- SDRAM
  - 512Mb : 64Mx8



SDRAM - Operation

- SDRAM
  - 512Mb : 32Mx16



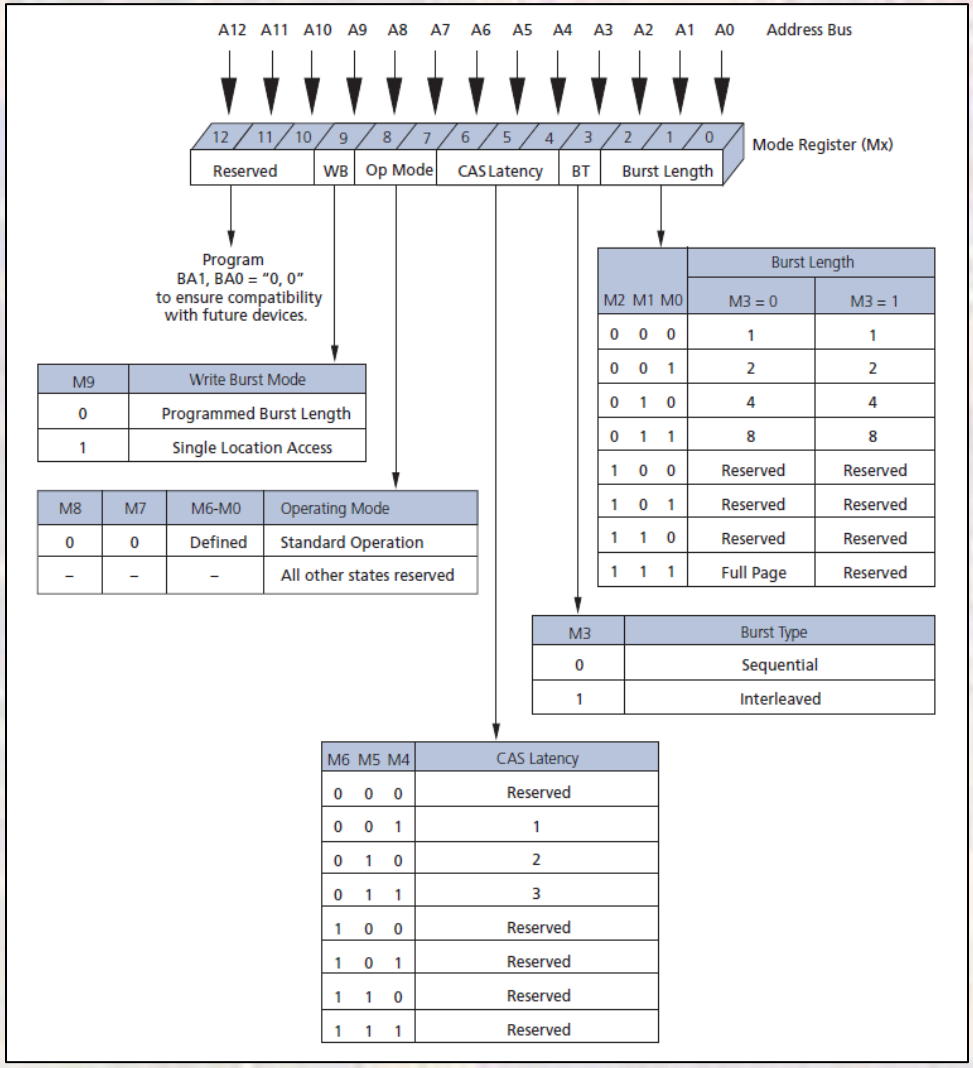
SDRAM - Operation

- SDRAM – Basic Commands
  - ACTIVATE – select 1 row in a specific bank (RAS) (open)
  - READ/WRITE – select a column (CAS)
  - PRECHARGE – prepare 1 or all banks for activation (close)
    - Auto precharge – automatically executes precharge after a Read or Write
  - Refresh / Auto Refresh
  - NOP – do nothing
  - Commands are decoded from the CS, RAS, CAS, and WE signals

Name (Function)	CS#	RAS#	CAS#	WE#	DQM	ADDR	DQ	Notes
COMMAND INHIBIT (NOP)	H	X	X	X	X	X	X	
NO OPERATION (NOP)	L	H	H	H	X	X	X	
ACTIVE (select bank and activate row)	L	L	H	H	X	Bank/row	X	2
READ (select bank and column, and start READ burst)	L	H	L	H	L/H	Bank/col	X	3
WRITE (select bank and column, and start WRITE burst)	L	H	L	L	L/H	Bank/col	Valid	3
BURST TERMINATE	L	H	H	L	X	X	Active	4
PRECHARGE (Deactivate row in bank or banks)	L	L	H	L	X	Code	X	5
AUTO REFRESH or SELF REFRESH (enter self refresh mode)	L	L	L	H	X	X	X	6, 7
LOAD MODE REGISTER	L	L	L	L	X	Op-code	X	8
Write enable/output enable	X	X	X	X	L	X	Active	9
Write inhibit/output High-Z	X	X	X	X	H	X	High-Z	9

SDRAM - Operation

- SDRAM – Programmable Modes



M9	Write Burst Mode
0	Programmed Burst Length
1	Single Location Access

M8	M7	M6-M0	Operating Mode
0	0	Defined	Standard Operation
–	–	–	All other states reserved

	Burst Length	
M2 M1 M0	M3 = 0	M3 = 1
0 0 0	1	1
0 0 1	2	2
0 1 0	4	4
0 1 1	8	8
1 0 0	Reserved	Reserved
1 0 1	Reserved	Reserved
1 1 0	Reserved	Reserved
1 1 1	Full Page	Reserved

M3	Burst Type
0	Sequential
1	Interleaved

M6 M5 M4	CAS Latency
0 0 0	Reserved
0 0 1	1
0 1 0	2
0 1 1	3
1 0 0	Reserved
1 0 1	Reserved
1 1 0	Reserved
1 1 1	Reserved

SDRAM - Operation

- SDRAM – Pins
  - Control

Symbol	Type	Description
CLK	Input	Clock: CLK is driven by the system clock. All SDRAM input signals are sampled on the positive edge of CLK. CLK also increments the internal burst counter and controls the output registers.
CKE	Input	Clock enable: CKE activates (HIGH) and deactivates (LOW) the CLK signal. Deactivating the clock provides precharge power-down and SELF REFRESH operation (all banks idle), active power-down (row active in any bank), or CLOCK SUSPEND operation (burst/access in progress). CKE is synchronous except after the device enters power-down and self refresh modes, where CKE becomes asynchronous until after exiting the same mode. The input buffers, including CLK, are disabled during power-down and self refresh modes, providing low standby power. CKE may be tied HIGH.
CS#	Input	Chip select: CS# enables (registered LOW) and disables (registered HIGH) the command decoder. All commands are masked when CS# is registered HIGH, but READ/WRITE bursts already in progress will continue, and DQM operation will retain its DQ mask capability while CS# is HIGH. CS# provides for external bank selection on systems with multiple banks. CS# is considered part of the command code.
CAS#, RAS#, WE#	Input	Command inputs: RAS#, CAS#, and WE# (along with CS#) define the command being entered.
BA[1:0]	Input	Bank address input(s): BA[1:0] define to which bank the ACTIVE, READ, WRITE, or PRECHARGE command is being applied.
A[12:0]	Input	Address inputs: A[12:0] are sampled during the ACTIVE command (row address A[12:0]) and READ or WRITE command (column address A[9:0], A11, and A12 for x4; A[9:0] and A11 for x8; A[9:0] for x16; with A10 defining auto precharge) to select one location out of the memory array in the respective bank. A10 is sampled during a PRECHARGE command to determine if all banks are to be precharged (A10 HIGH) or bank selected by A10 (LOW). The address inputs also provide the op-code during a LOAD MODE REGISTER command.

SDRAM - Operation

- SDRAM – Pins
  - Data

Symbol	Type	Description
x16: DQ[15:0]	I/O	Data input/output: Data bus for x16 (pins 4, 7, 10, 13, 15, 42, 45, 48, and 51 are NC for x8; and pins 2, 4, 7, 8, 10, 13, 15, 42, 45, 47, 48, 51, and 53 are NC for x4).
x8: DQ[7:0]	I/O	Data input/output: Data bus for x8 (pins 2, 8, 47, 53 are NC for x4).
x4: DQ[3:0]	I/O	Data input/output: Data bus for x4.
x4, x8: DQM x16: DQML, DQMH LDQM, UDQM (54-ball)	Input	Input/output mask: DQM is an input mask signal for write accesses and an output enable signal for read accesses. Input data is masked when DQM is sampled HIGH during a WRITE cycle. The output buffers are placed in a High-Z state (two-clock latency) when DQM is sampled HIGH during a READ cycle. On the x4 and x8, DQML (pin 15) is a NC and DQMH is DQM. On the x16, DQML corresponds to DQ[7:0], and DQMH corresponds to DQ[15:8]. DQML and DQMH are considered same state when referenced as DQM.

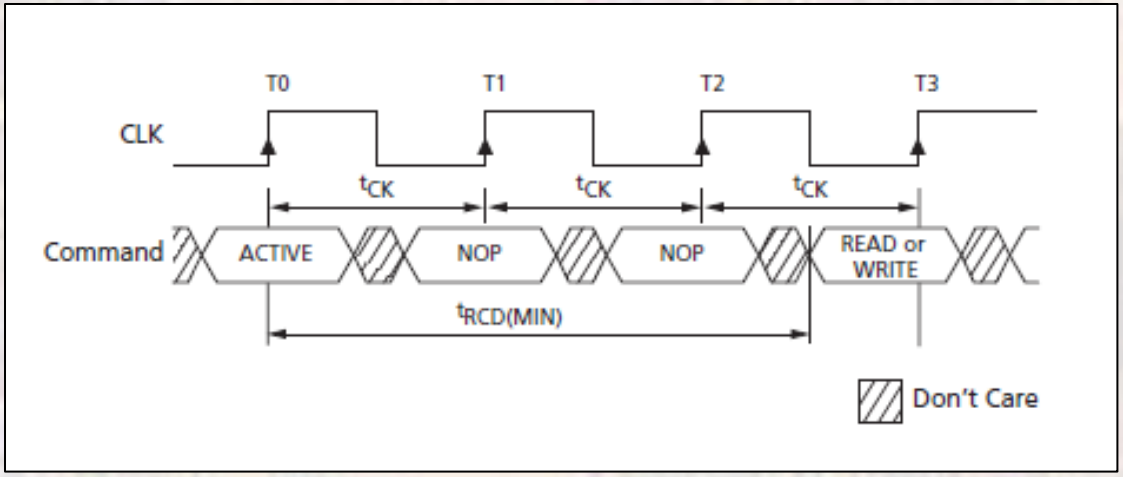
SDRAM - Operation

- SDRAM – Pins
  - Power

Symbol	Type	Description
V_{DDQ}	Supply	DQ power: DQ power to the die for improved noise immunity.
V_{SSQ}	Supply	DQ ground: DQ ground to the die for improved noise immunity.
V_{DD}	Supply	Power supply: +3.3V ±0.3V.
V_{SS}	Supply	Ground.
NC	–	These should be left unconnected.

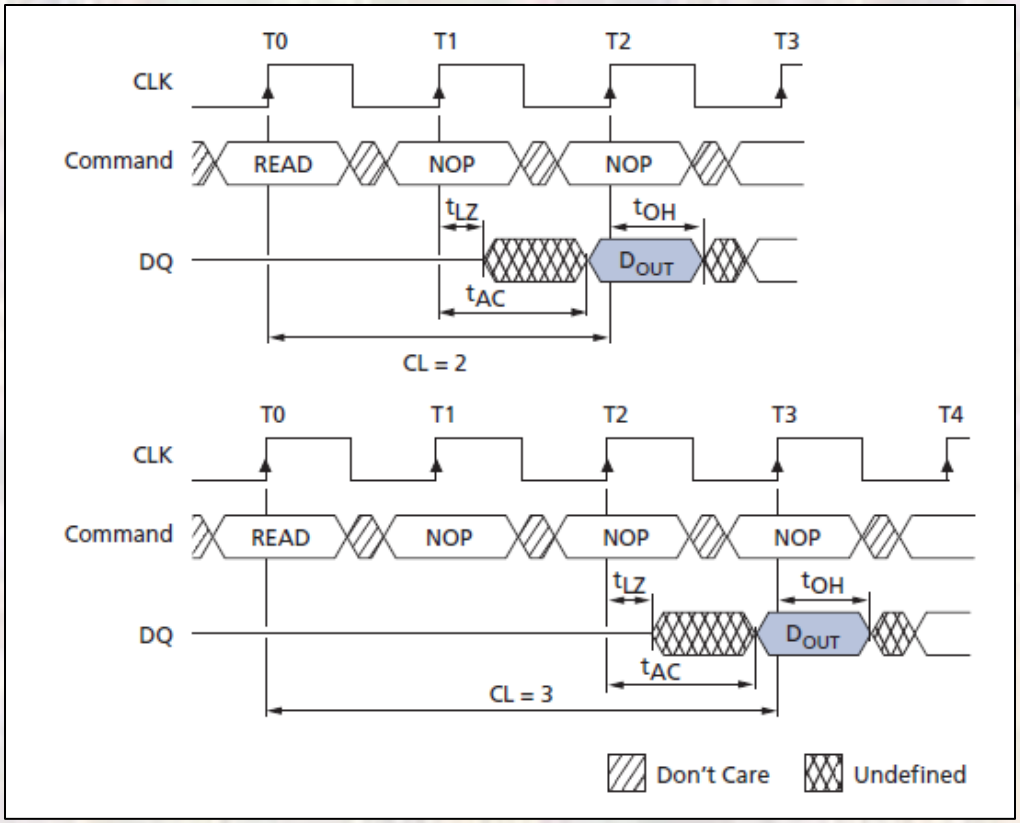
SDRAM - Operation

- SDRAM – Timing
  - Bank/Row Activation
    - Min time from Activate (RAS) to read/write command
    - $T_{RCD(min)}$



SDRAM - Operation

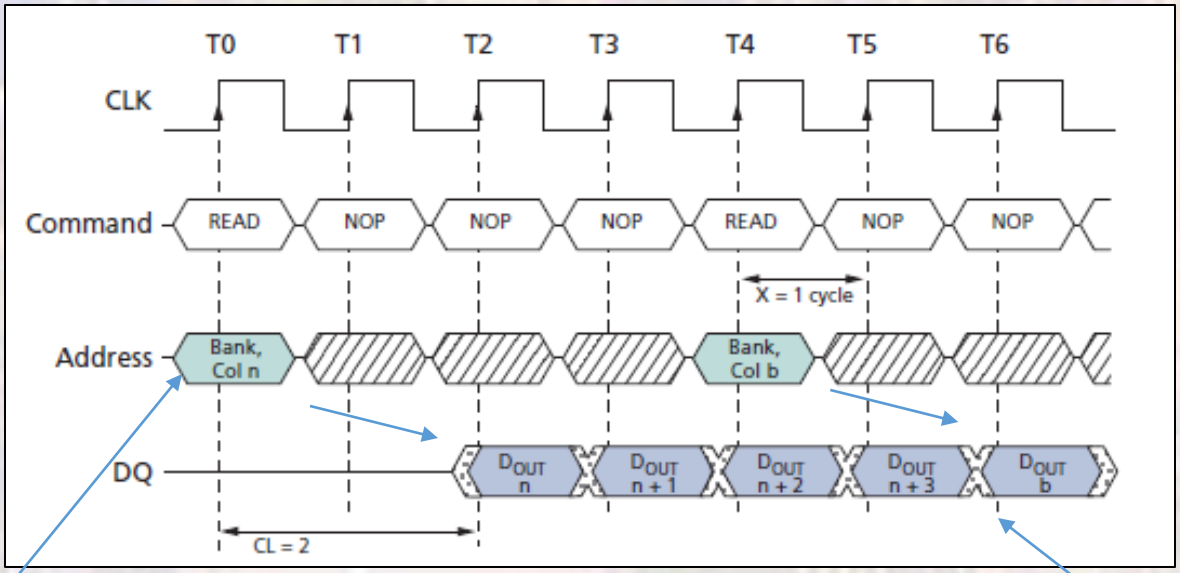
- SDRAM – Timing
  - CAS – Latency
    - # of clocks from read/write to valid read data
    - CL



SDRAM - Operation

- SDRAM – Timing
  - Read
    - BL = 4 (burst length)

Assumes Activate Completed



Note: must keep bank selected at the read command clk edge

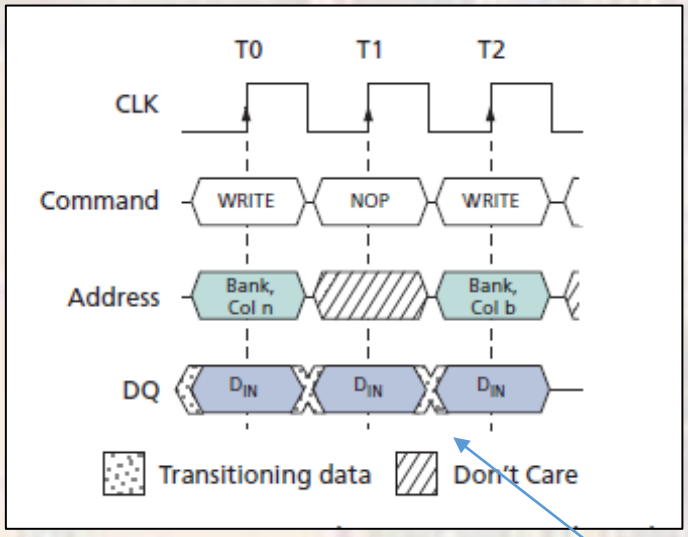
1 read command
1 read address
burst of 4 outputs

0 output data cycles lost

SDRAM - Operation

- SDRAM – Timing
  - Write
    - BL = 2
    - No CAS latency, data is latched in an input buffer

Assumes Activate Completed



Data must be stable on write command Clk edge

Note: must keep bank selected at the read command clk edge

0 input data cycles lost

1 write command
1 write address
burst of 2 inputs