

# Memory Topology Logical

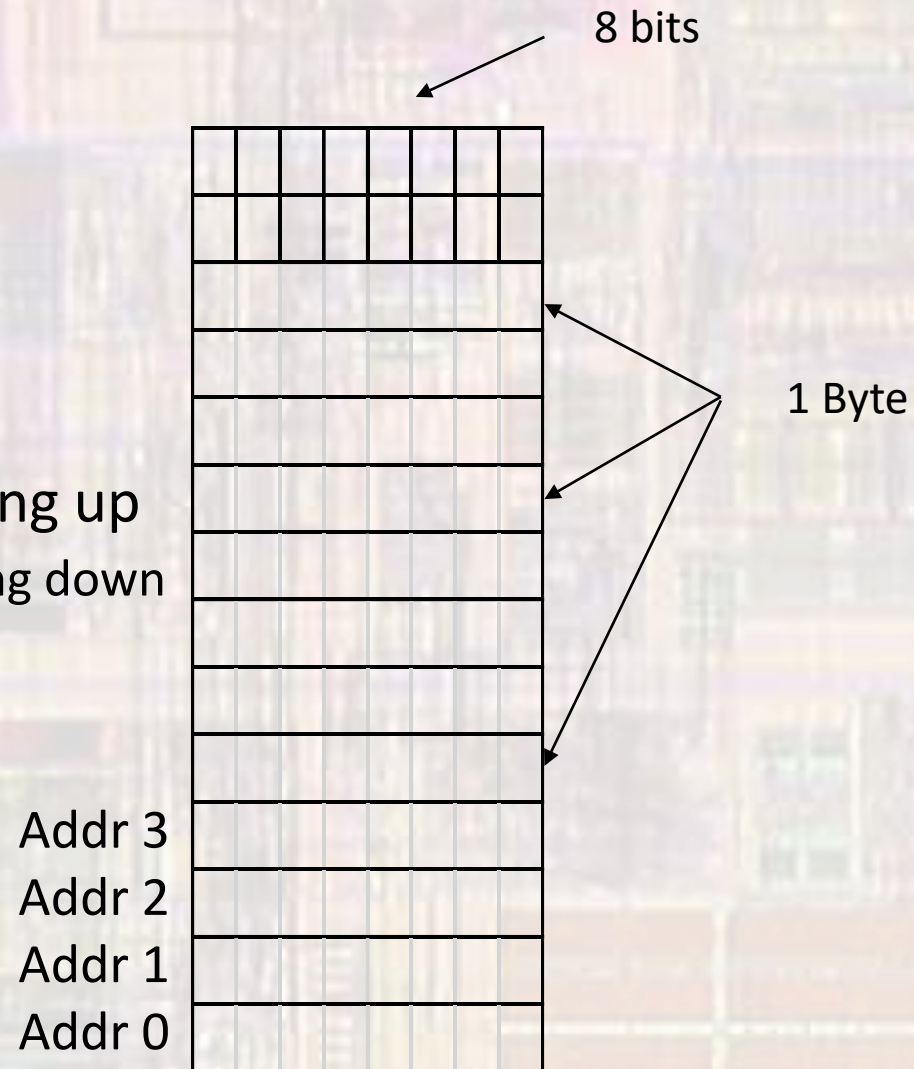
Last updated 2/1/24

# Memory Topology – Logical

- Elements
  - Minimum logical element
    - 1 – bit (b)
    - Has a logical value of '0' or '1'
    - Has a physical value of “vdd” or “gnd”
      - 5v, 3.3v, 2.4v, 1.8v, 1.2v
  - Minimum accessible storage element
    - 1- Byte (B)
    - 8 bits
  - Minimum Addressable element
    - 1 – Word
    - Situational dependent length
    - 1B, 2B, 4B, 8B, 16B, ...

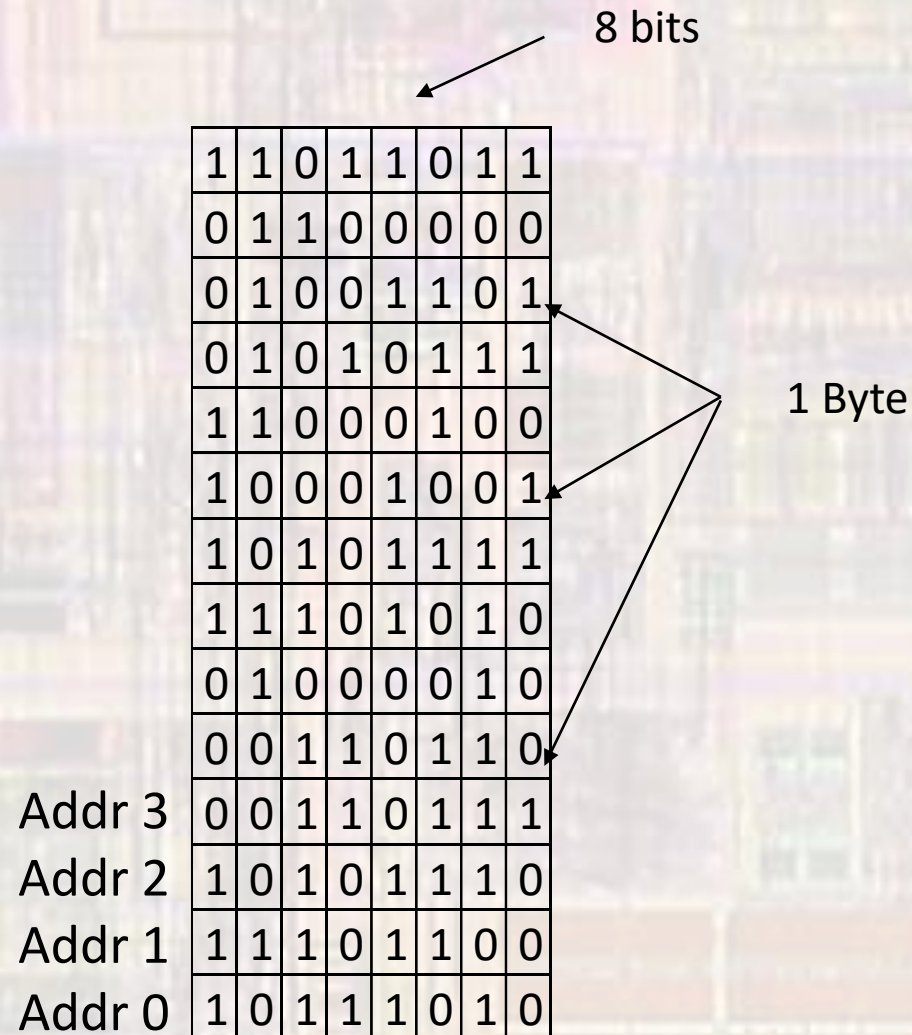
# Memory Topology – Logical

- Logical configuration
  - Long column of **bytes**
  - 1<sup>st</sup> address is “0”
  - Typically thought of as growing up
    - Sometimes thought of as growing down



# Memory Topology – Logical

- Initialization
  - Even though we may not have stored anything in a specific memory location
    - It has a value
    - The value is likely random



# Memory Topology – Logical

- Write
  - Provide Address and Data
  - Write (addr 4, 11101000)
  - Write (addr 6, 00000101)
  - Write (addr 10, 11001010)
  - Note: **Writing overwrites existing data**

	0	0	1	0	0	1	1	1
	1	1	1	0	1	0	0	0
	0	0	0	1	1	1	0	1
	1	1	0	0	1	0	1	0
	0	1	1	1	1	0	1	1
	0	0	0	1	0	0	0	1
	0	0	0	1	1	1	0	1
	0	0	0	0	0	1	0	1
	1	0	1	1	0	1	0	0
	1	1	1	0	1	0	0	0
Addr 3	1	0	0	1	0	1	1	1
Addr 2	1	1	0	1	1	1	0	1
Addr 1	1	1	0	1	0	1	0	0
Addr 0	1	0	1	0	1	0	0	1

# Memory Topology – Logical

- Read

- Provide Address

- Read (addr 4) → 11101000

- Read (addr 6) → 00000101

- Read (addr 8) → ????????

- NOTE: **Reading does not destroy the data**

	0	0	1	0	0	1	1	1
	1	1	1	0	1	0	0	0
	0	0	0	1	1	1	0	1
	1	1	0	0	1	0	1	0
	0	1	1	1	1	0	1	1
	0	0	0	1	0	0	0	1
	0	0	0	1	1	1	0	1
	0	0	0	0	0	1	0	1
	1	0	1	1	0	1	0	0
	1	1	1	0	1	0	0	0
Addr 3	1	0	0	1	0	1	1	1
Addr 2	1	1	0	1	1	1	0	1
Addr 1	1	1	0	1	0	1	0	0
Addr 0	1	0	1	0	1	0	0	1

# Memory Topology – Logical

- Addresses

- Addresses are **NOT** part of the memory array
- Addresses are logic circuits to choose which part of the array to read from or write to – **decoders determine the location**

0	0	1	0	0	1	1	1
1	1	1	0	1	0	0	0
0	0	0	1	1	1	0	1
1	1	0	0	1	0	1	0
0	1	1	1	1	0	1	1
0	0	0	1	0	0	0	1
0	0	0	1	1	1	0	1
0	0	0	0	0	1	0	1
1	0	1	1	0	1	0	0
1	1	1	0	1	0	0	0
1	0	0	1	0	1	1	1
1	1	0	1	1	1	0	1
1	1	0	1	0	1	0	0
1	0	1	0	1	0	0	1

Addr 3

Addr 2

Addr 1

Addr 0

# Memory Topology – Logical

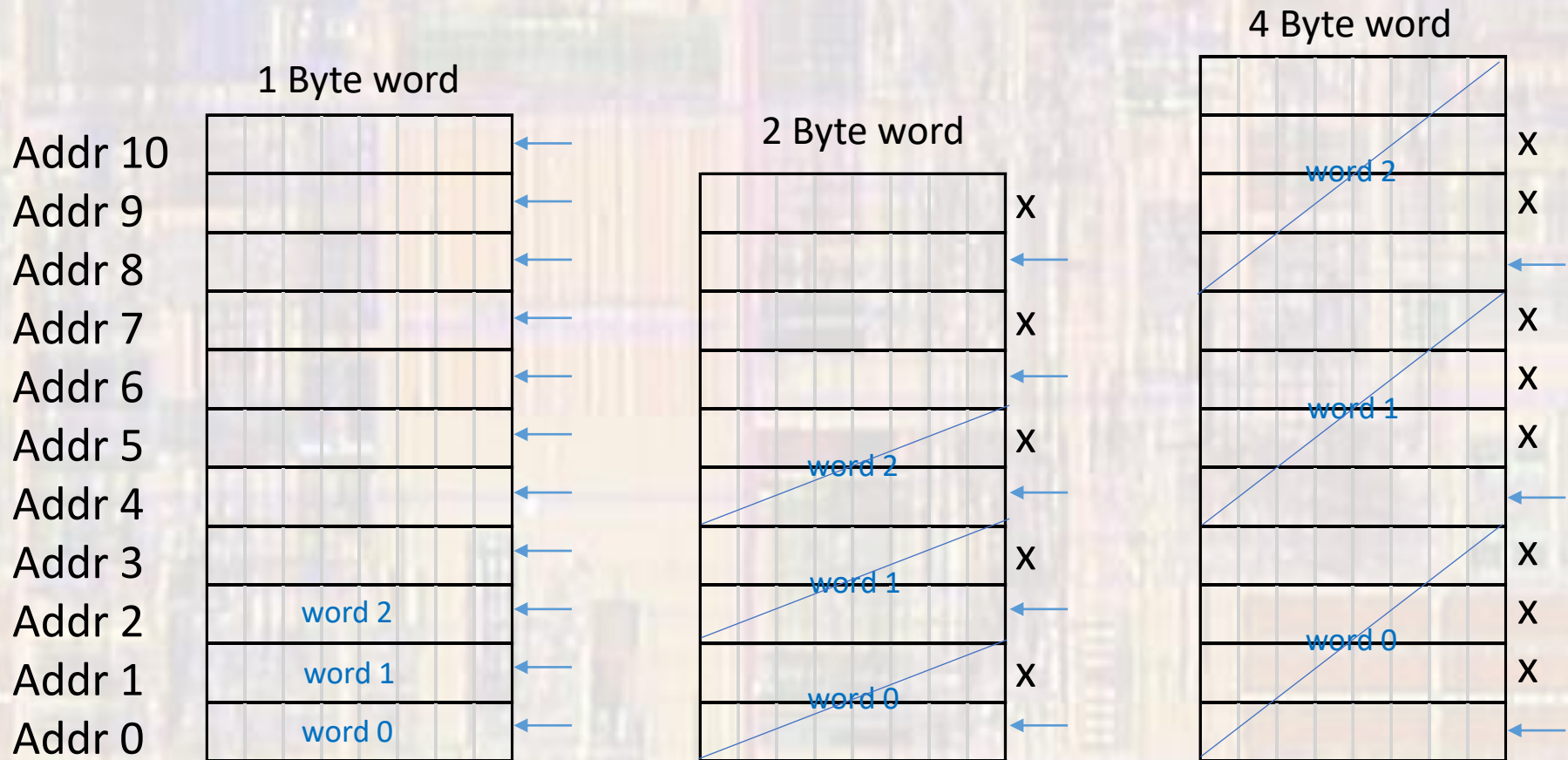
- Word Alignment
  - Processors work with data WORDS
  - Size of the internal registers
    - 1 Byte – 8 bit processor
    - 2 Bytes – 16 bit processor
    - 4 Bytes – 32 bit processor
    - 8 Bytes – 64 bit processor
  - Memory is word aligned
    - Must access the entire word
    - Not allowed/possible to access inside a word\*

\* exceptions exist



# Memory Topology – Logical

- Word Alignment
  - Allowed addresses indicated by ←



# Memory Topology – Logical

- Endianness

- The order words > 1B are stored in memory
- data value 01110111 10111011 11011101 01110111 in a 4 byte word

