# Memory Topology Physical

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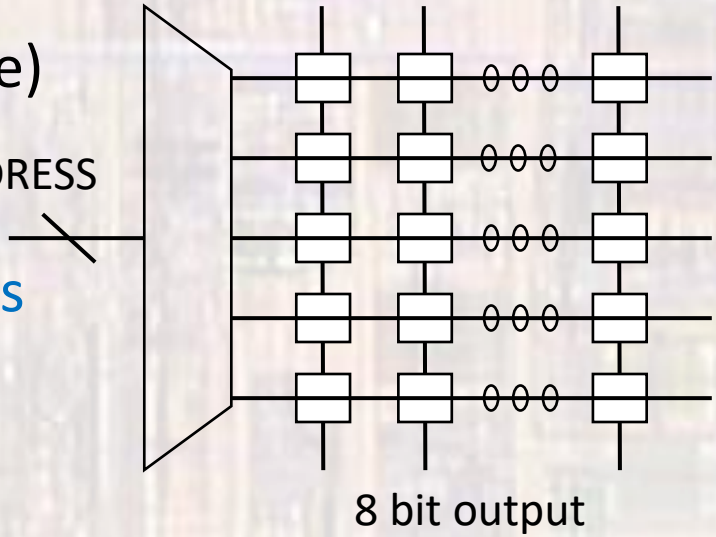
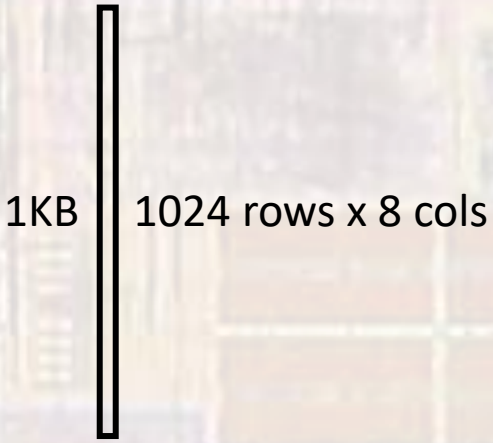
# Memory Topology - Physical

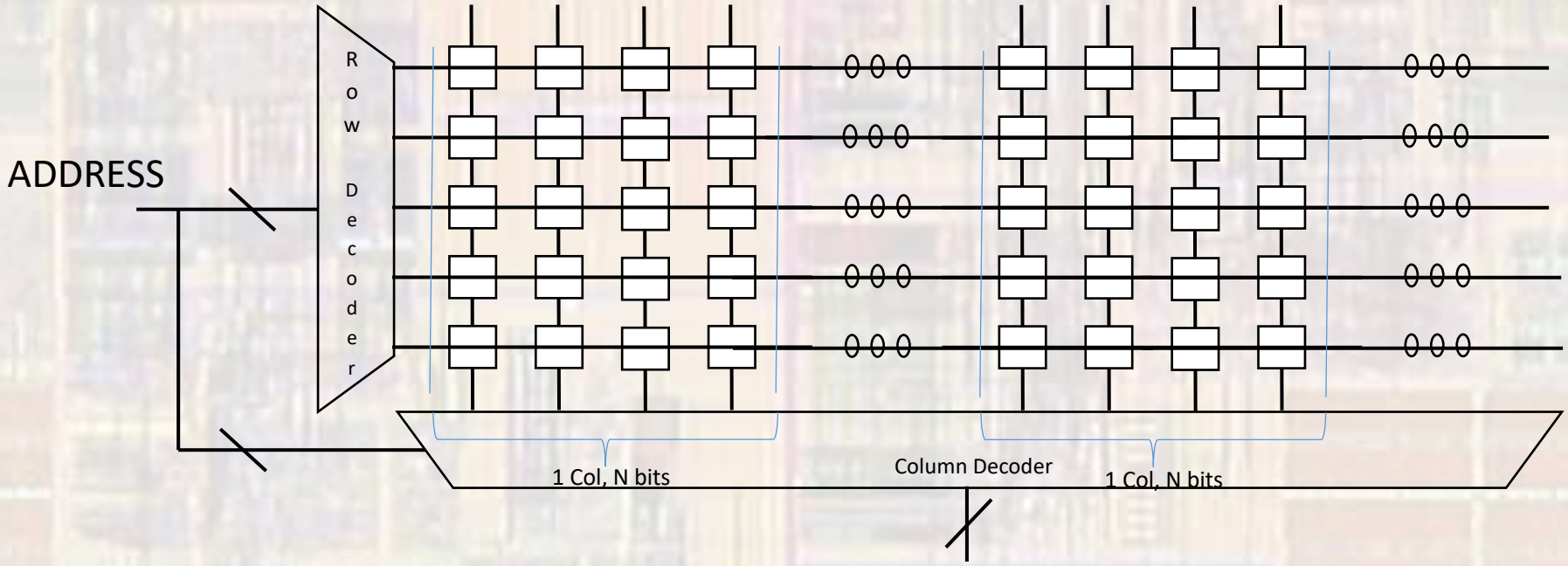
- Direct implementation of the Logical view
  - Array of single bit cells (8 bits wide)
  - Row decoder chooses 1 row
  - Rows are typically called wordlines
  - Bit Cell Columns are typically called bitlines
  - Non optimal
    - Physical implementation
      - Non-practical die dimensions
    - Speed
      - Long lines → slow speeds



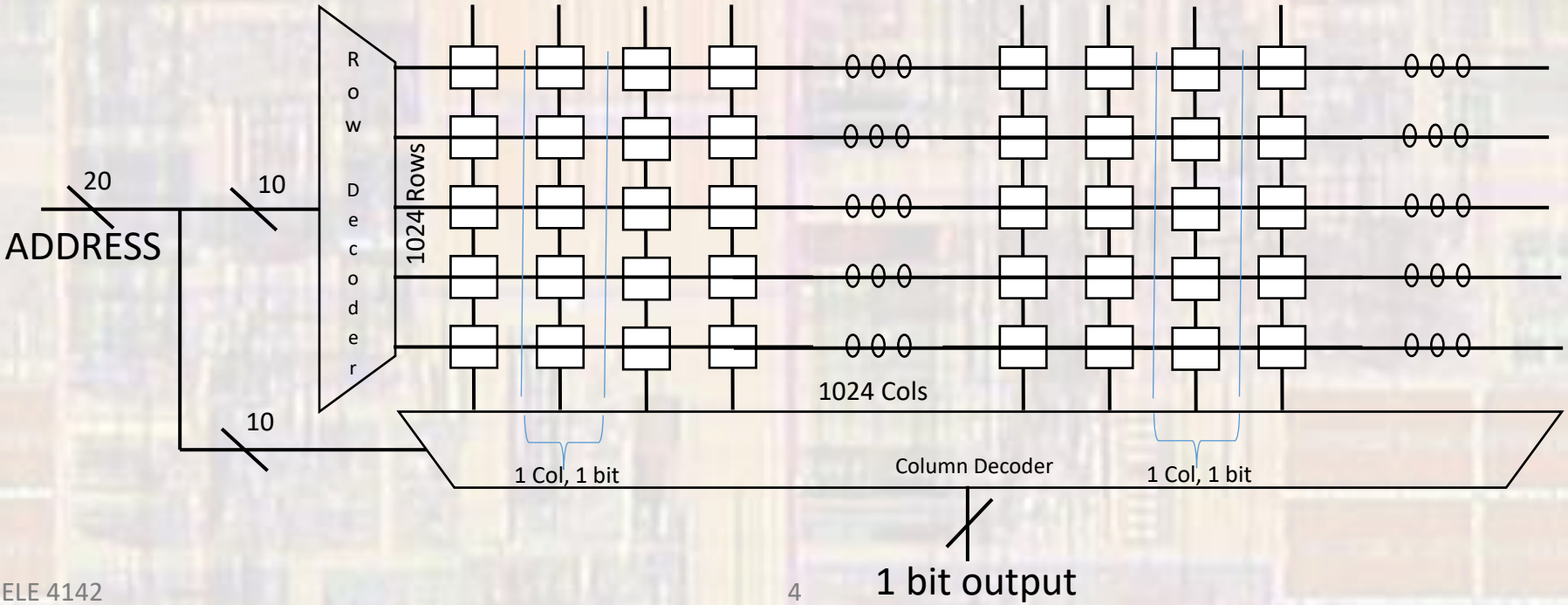
# Memory Topology - Physical

- Practical Physical Structure
  - Array of single bit cells
    - Typically, square <-> 1::2 ratio
    - Grouped as N bit columns
    - N = 1,4,8,16,32,64,128,… bits/column
  - Row decoder chooses 1 row
  - Column decoder chooses 1 column



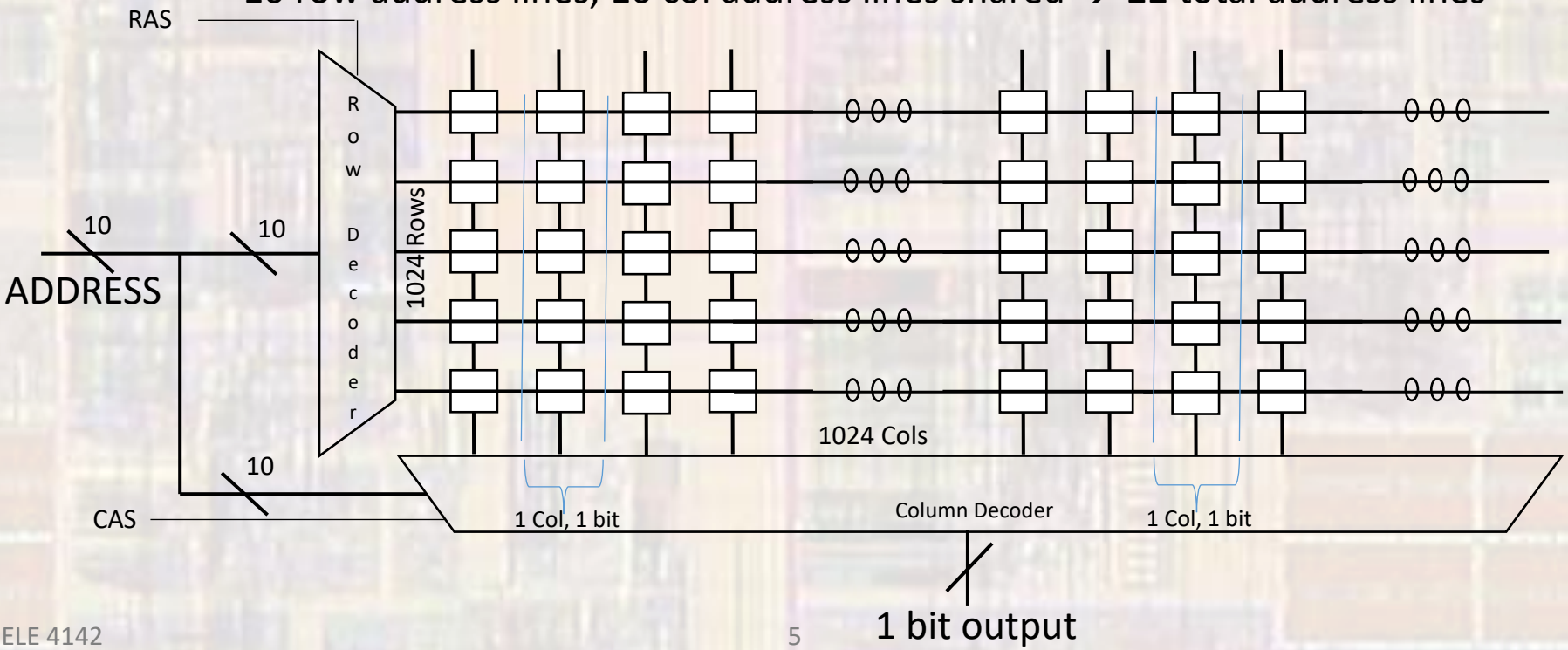
# Memory Topology - Physical

- Practical Physical Structure
  - 1Mb array, with square bit cells, in a x1 (col = 1bit) architecture
    - 1K rows X 1K columns
    - 10 row address lines, 10 col address lines → 20 total address lines



# Memory Topology - Physical

- Practical Physical Structure
  - 1Mb array, with square bit cells, in a x1 (col = 1bit) architecture – with shared address lines
    - 1K rows X 1K columns
    - Add a Row Address Strobe (RAS) and Column Address Strobe (CAS)
      - Row decode is active when RAS high, Col decode is active when CAS high
    - 10 row address lines, 10 col address lines shared → 22 total address lines

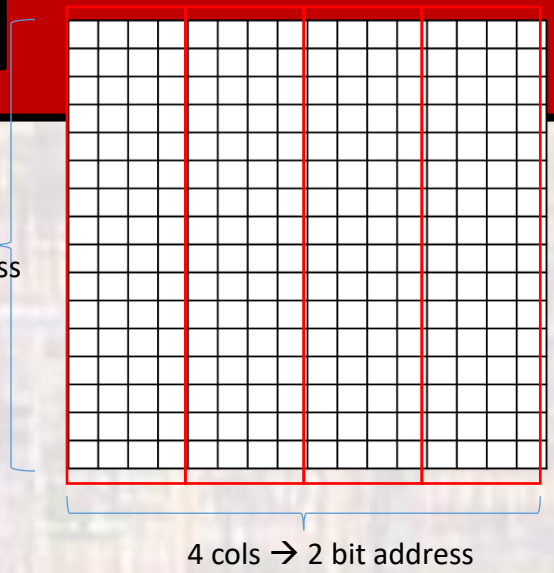


# Memory Topology - Physical

- Memory Descriptive Terminology
  - 16Mb in a x4
    - 16Mb total memory, each memory address provides 4 bits
  - 16Mb x 4
    - 64Mb total memory, each memory address provides 4 bits
    - Could be configured as 4 16MB memories, each providing 1b to the output

# Memory Topology - Physical

- Memory Descriptive Terminology
  - Example – 16Mb in a x4 configuration
    - address sharing




16Mb total → 16,777,216 bits
x4 means each column is 4 bits
or each address points to 4 bits

16Mb in a x4 configuration → 4 bits / address → 4,194,304 - individual addresses
→ 22 total address bits

Assuming a square memory array and a square bit cell → 4 times as many rows as columns
4 times as many rows as columns → 2 more row address bits than column address bits

22 address bits → 12 bits for row addresses and 10 bits for column addresses

IF sharing address bits → 12 address bits + RAS + CAS = 14 total address signals

# Memory Topology - Physical

- Memory Packaging
  - Single chip
    - DIP, SOP, BGA
  - SIMM
    - Single In-line Memory Module
    - 4Mb Module → 8, 256Kb x 1 chips
    - 32b processor would require 4 SIMMs
  - DIMM
    - Dual In-line Memory Module
    - 2 sided version of a SIMM, thicker but shorter
  - DDRx
    - Double Data rate (SDRAM)
    - DIMM with registration slots tied to DDRx type