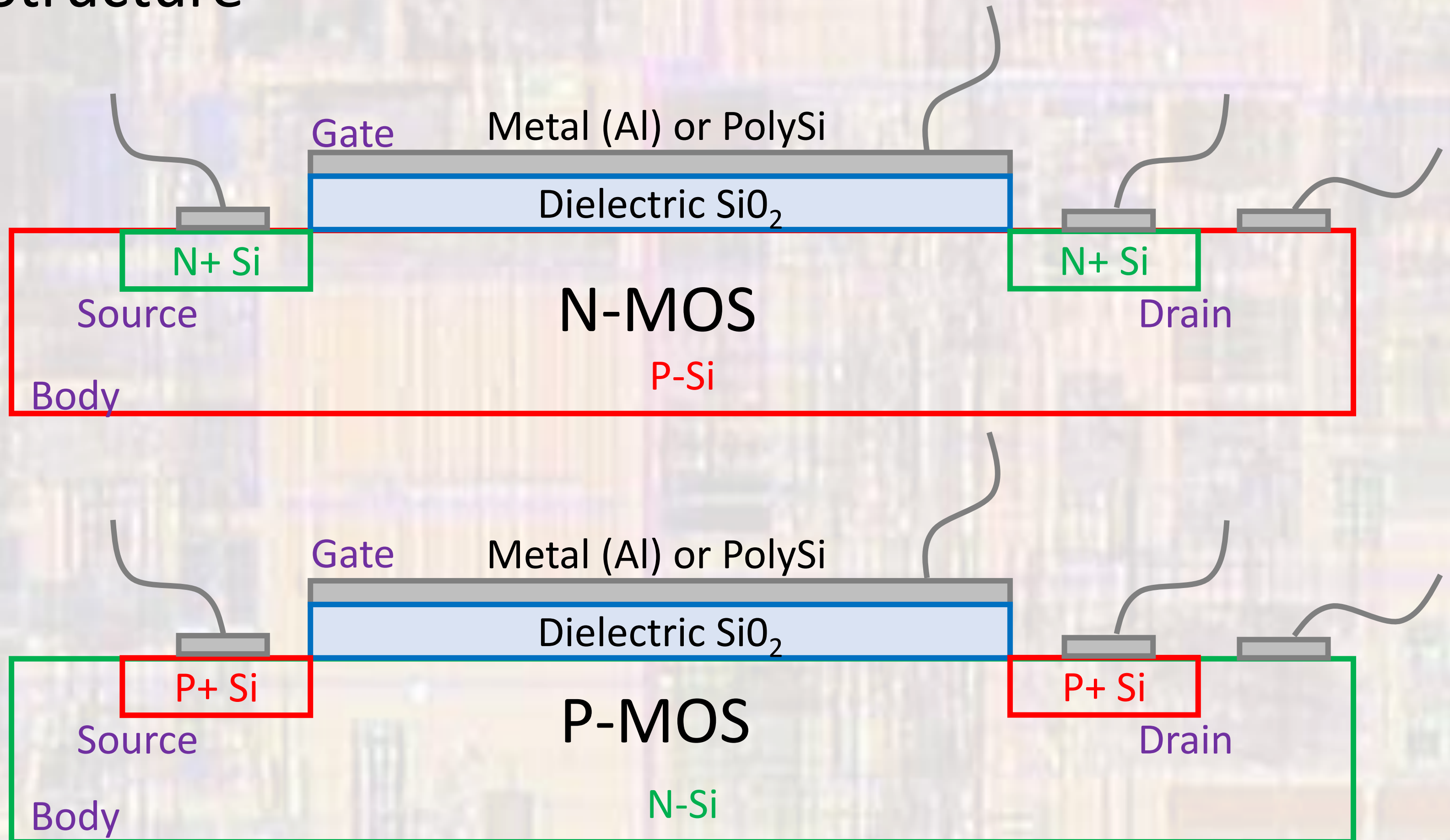
MOS Transistors

Last updated 1/11/24

MOS Enhancement Mode Transistor

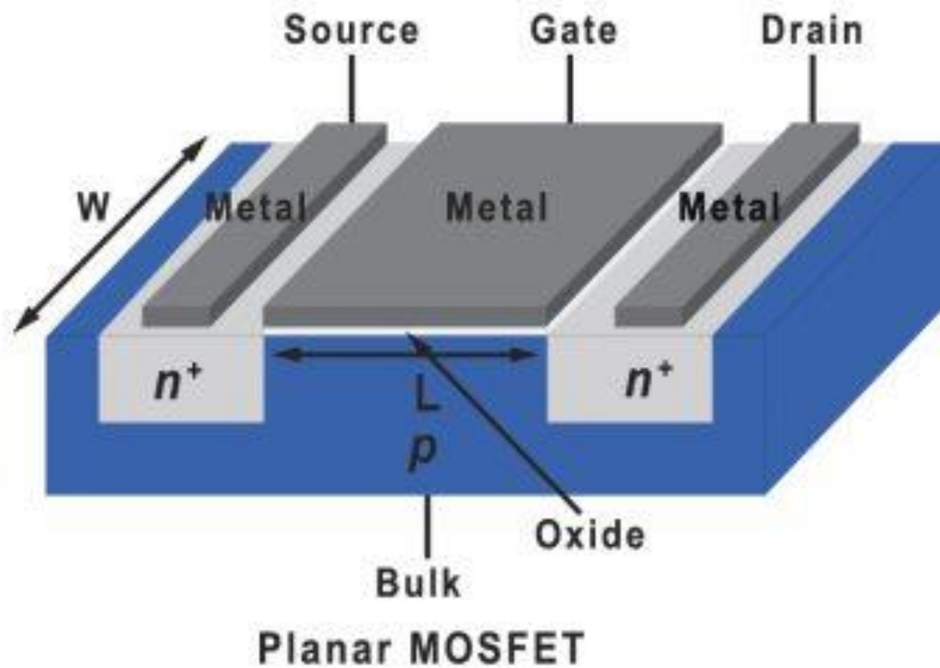
- Structure



© tj

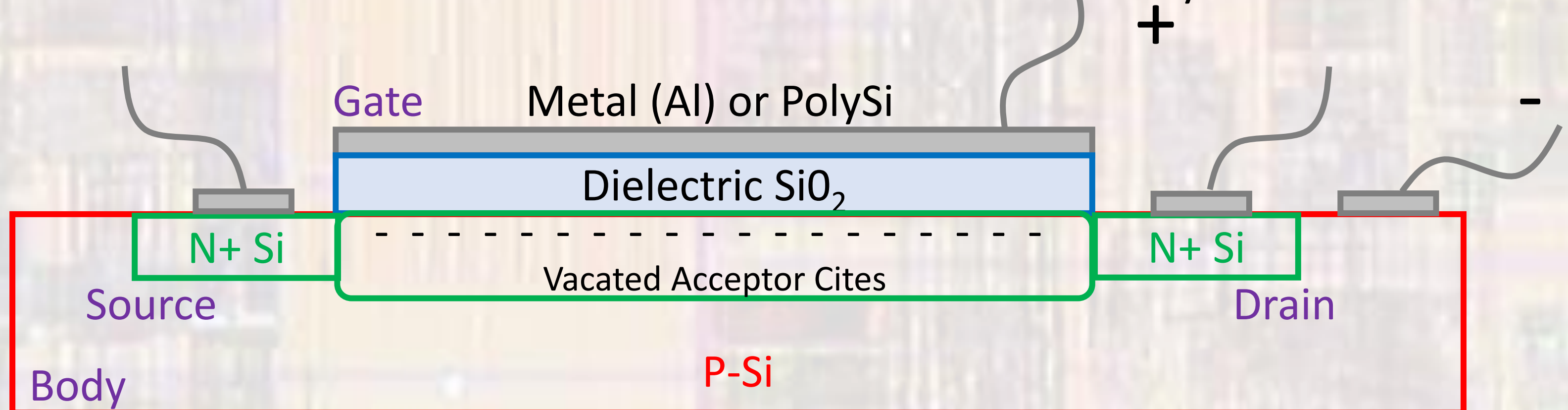
MOS Enhancement Mode Transistor

- Structure



MOS Enhancement Mode Transistor

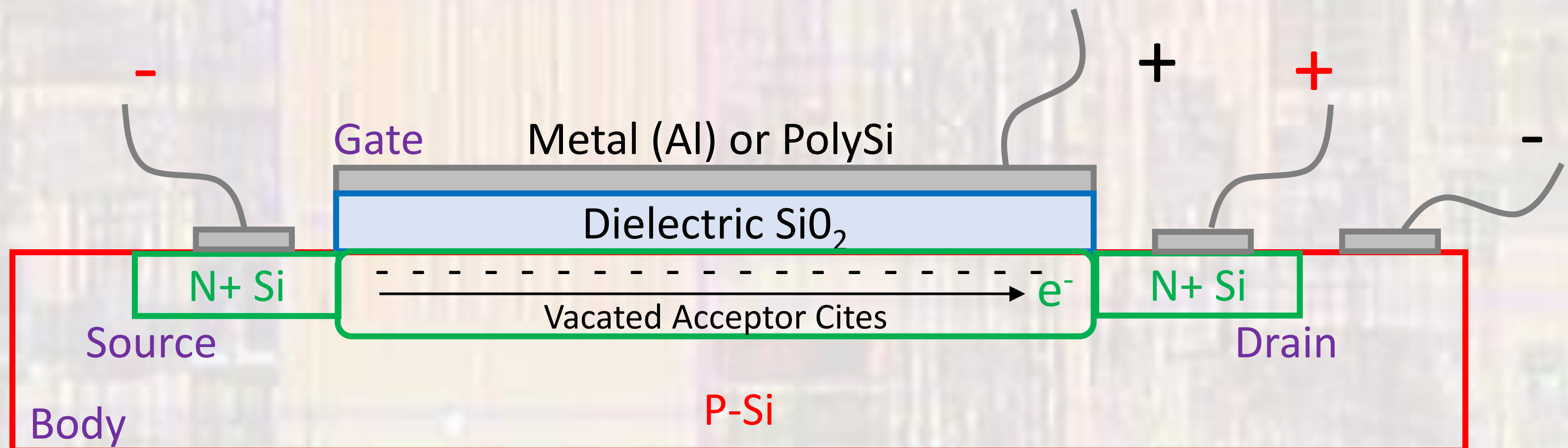
- N-MOS Operation
  - Large Positive Bias
    - Depletion region is formed
      - Mobile holes pushed away (region is depleted of holes)
      - Net negative (fixed) charge left behind
      - Electrons are drawn from the Si to form an inversion layer



A channel is formed from Source to Drain
Electrons can flow through this channel

MOS Enhancement Mode Transistor

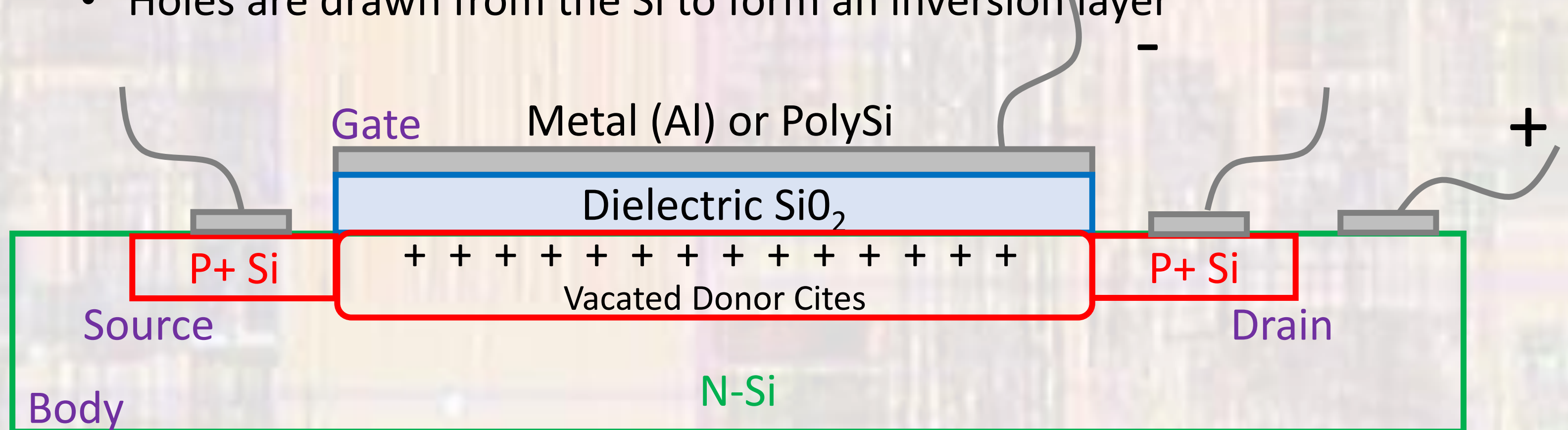
- N-MOS Operation
  - Large Positive Bias + Positive Bias from Drain to Source
    - Electrons move from Source to Drain
    - Current flows from Drain to Source



© tj

MOS Enhancement Mode Transistor

- P-MOS Operation
  - Large Negative Bias
    - Depletion region is formed
      - Mobile electrons pushed away (region is depleted of electrons)
      - Net positive (fixed) charge left behind
      - Holes are drawn from the Si to form an inversion layer

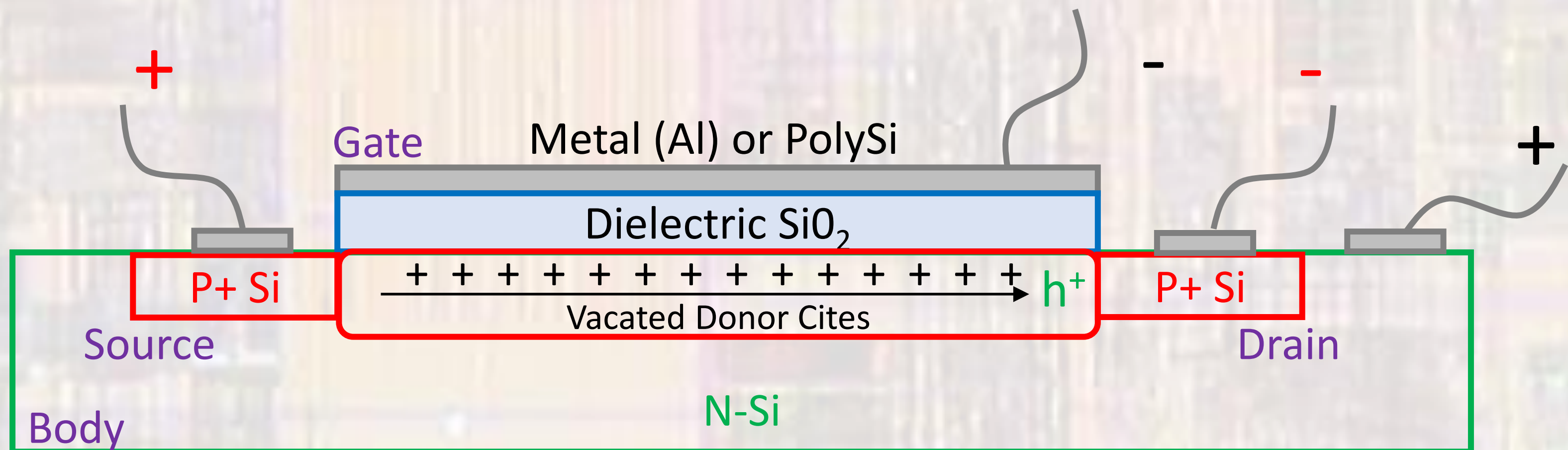


A channel is formed from Source to Drain
Holes can flow through this channel

© tj

MOS Enhancement Mode Transistor

- P-MOS Operation
  - Large Negative Bias + Positive Bias from Source to Drain
    - Holes move from Source to Drain
    - Current flows from Source to Drain



MOS Enhancement Mode Transistor

- Parameters
  - W – width of the transistor
  - L – length of the transistor (S to D)
  - V_{th} – threshold voltage (inversion layer formed)
  - Kn, Kp – conduction parameter

$$K_n = \frac{W\mu_n C_{ox}}{2L} \qquad K_p = \frac{W\mu_p C_{ox}}{2L}$$

$$K_n = \frac{k'_n}{2}\frac{W}{L} \qquad K_p = \frac{k'_p}{2}\frac{W}{L}$$

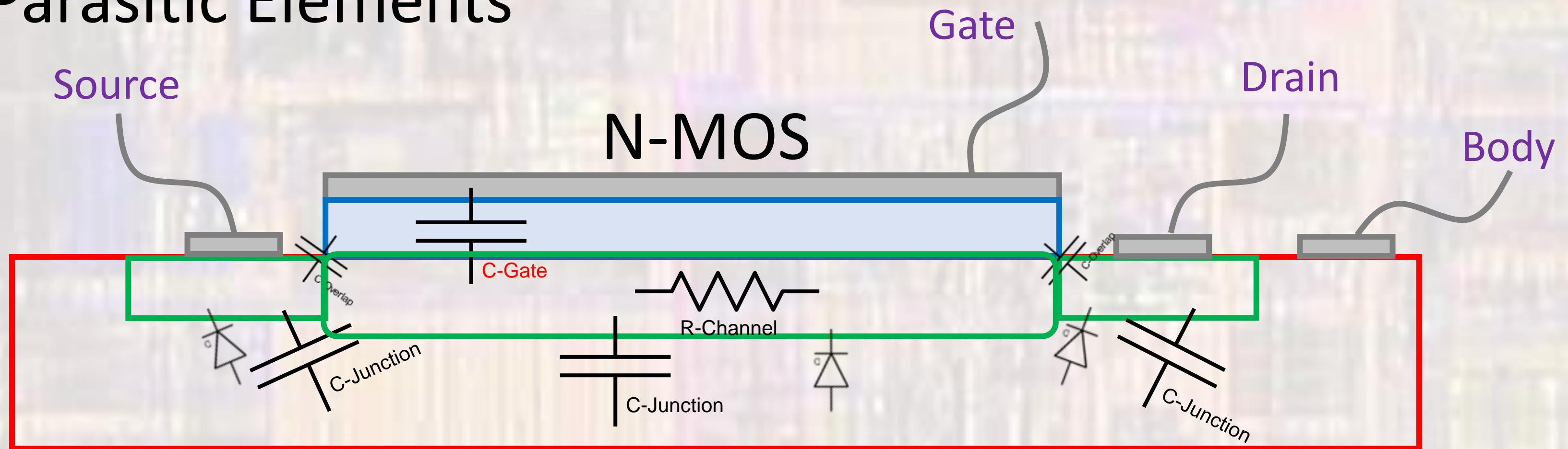
$$k'_n = \mu_n C_{ox} \qquad k'_p = \mu_p C_{ox}$$

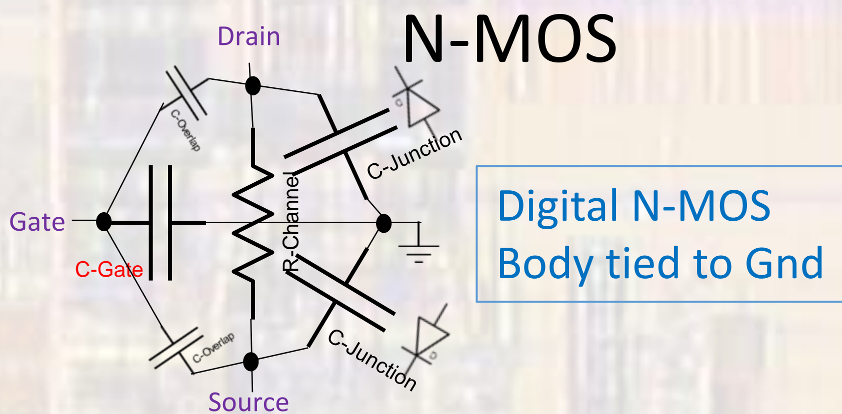
μ_n, μ_n, C_{ox} fixed for a given semiconductor process

© tj

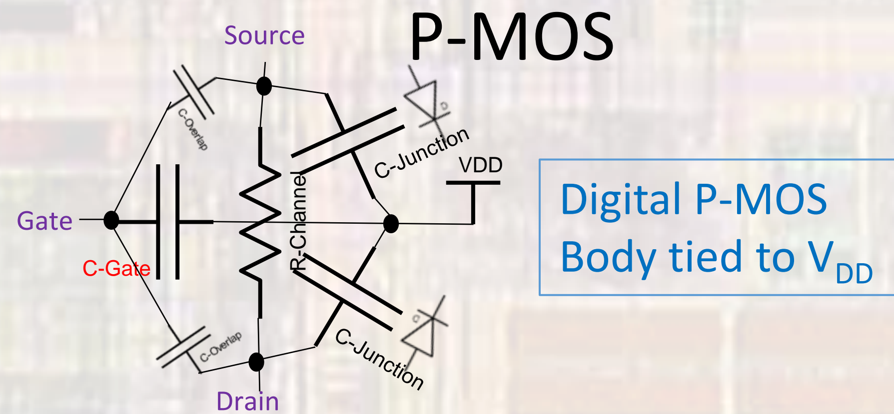
MOS Enhancement Mode Transistor

- Parasitic Elements





Digital N-MOS
Body tied to Gnd



Digital P-MOS
Body tied to V_{DD}

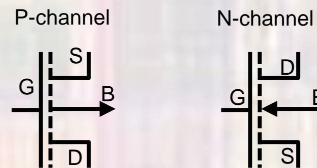
© tj

MOS Enhancement Mode Transistor

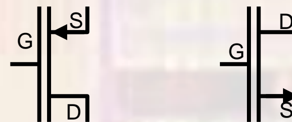
- Parasitic Elements
  - Gate
    - Capacitive
    - No DC current
    - AC/Transient current
  - S/D
    - Channel – Resistive
      - Dependent on V_{GS} and V_{DS}
    - Capacitive to Gnd (V_{DD})
      - No DC current
      - AC/Transient current
    - Reverse Biased Diode to Gnd (V_{DD})
      - Small leakage current independent of transistor action

MOS Enhancement Mode Transistor

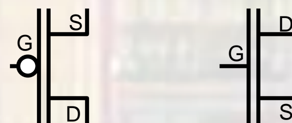
- Enhancement Mode
  - A bias is required to form the channel
  - 4-terminal symbol



  - In digital applications the Source is typically tied to
    - Vdd for P-MOS
    - Gnd for N-MOS



  - The simplified logic symbols

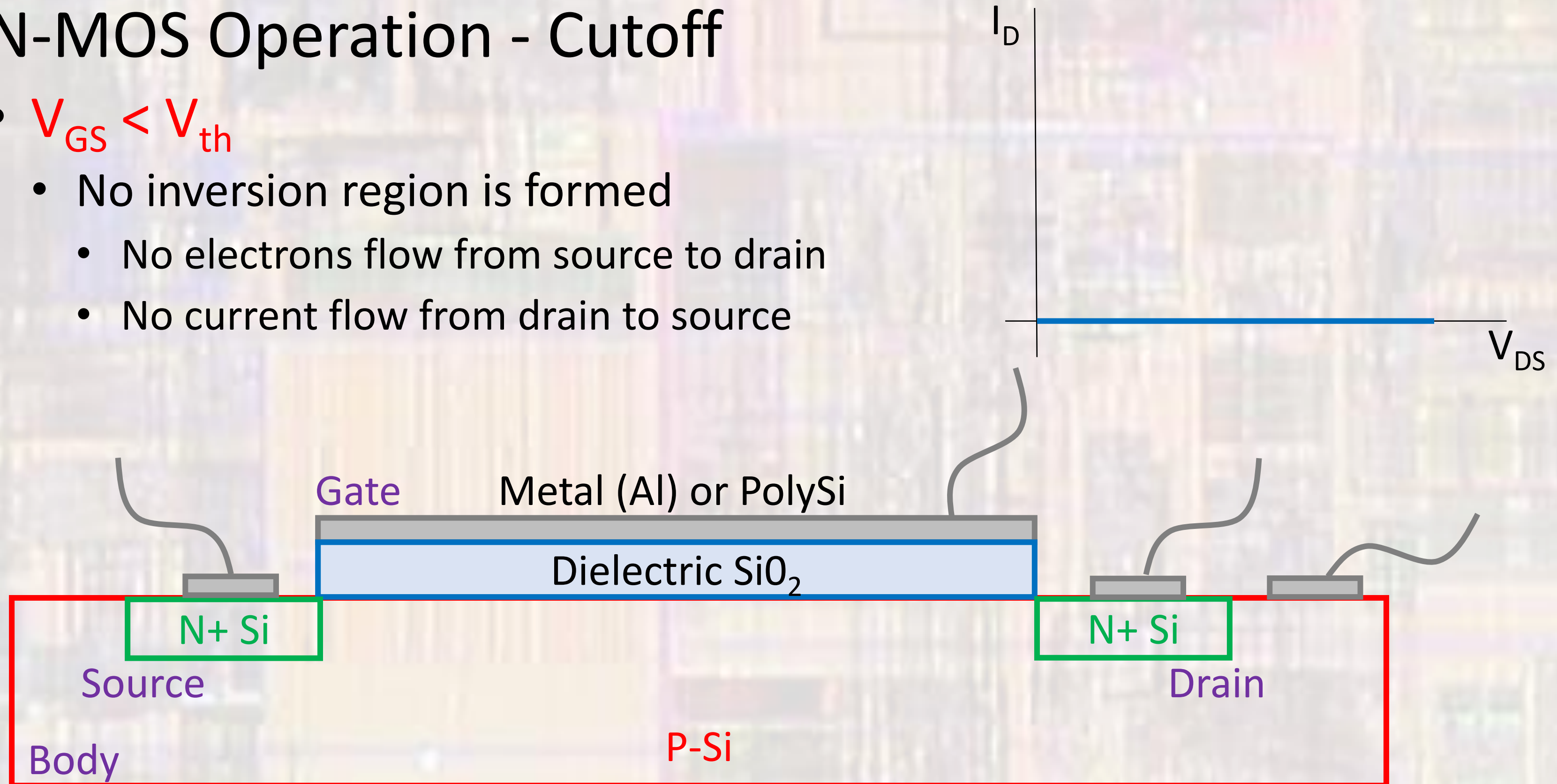


Note – almost all N-MOS and P-MOS devices used today are enhancement mode – so the dashed line is omitted

© tj

MOS I-V Characteristics

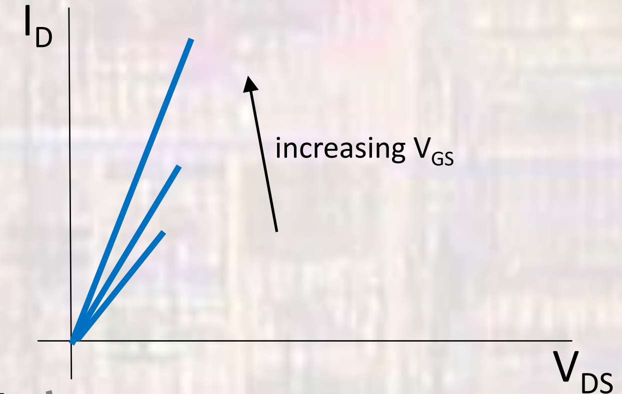
- N-MOS Operation - Cutoff
  - $V_{GS} < V_{th}$
    - No inversion region is formed
      - No electrons flow from source to drain
      - No current flow from drain to source

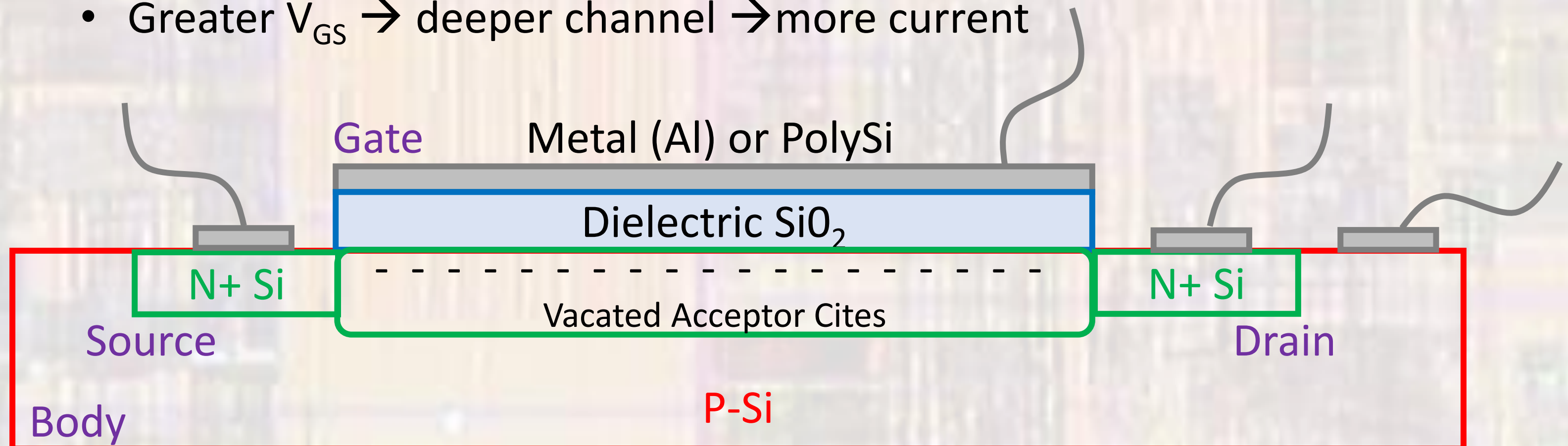


$$I_D = 0$$

MOS I-V Characteristics

- N-MOS Operation – Linear
  - $V_{GS} > V_{th}$, $V_{DS} < V_{DSsat}$
    - Inversion region is formed
      - Electrons can flow from source to drain
      - Current can flow from drain to source
      - Greater V_{GS} → deeper channel → more current





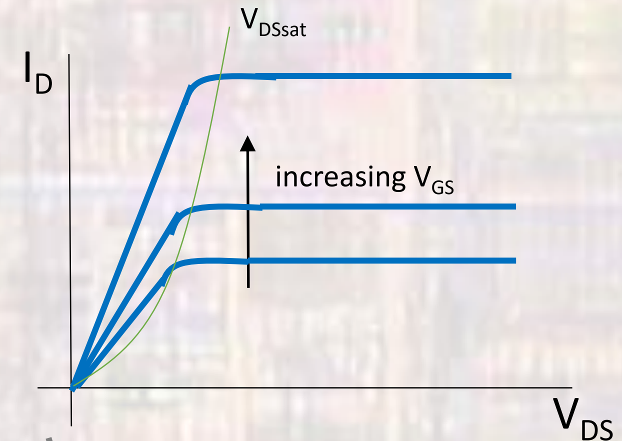
$V_{DSsat} = V_{GS} - V_{th}$

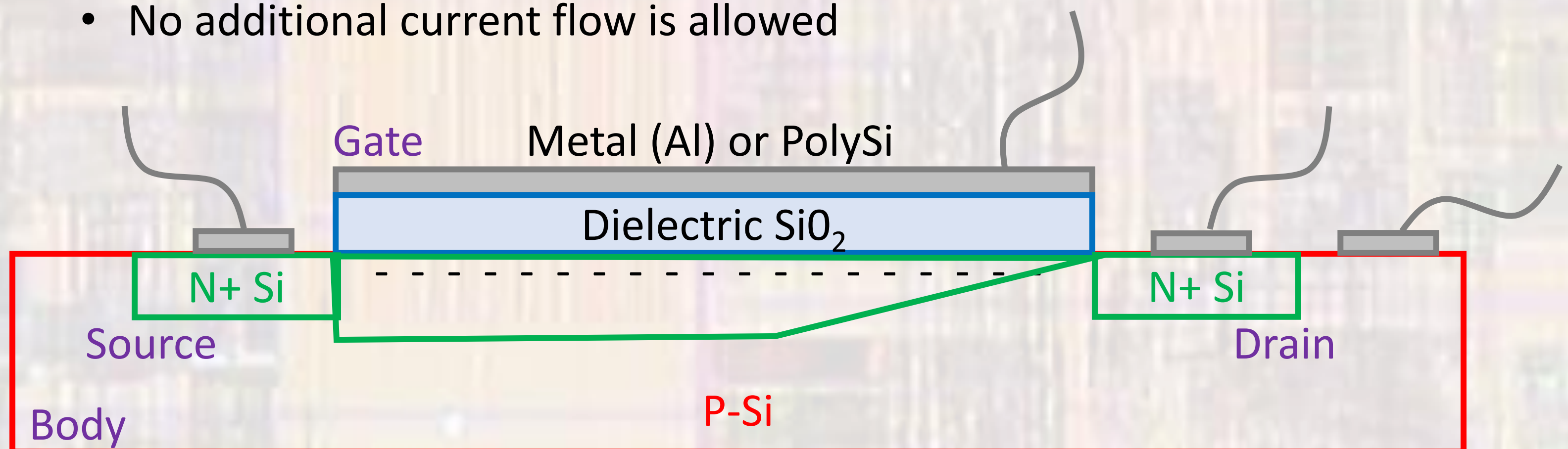
$$I_D = K_n[2(V_{GS} - V_{tn})V_{DS} - V_{DS}^2]$$

© tj

MOS I-V Characteristics

- N-MOS Operation – Saturation
  - $V_{GS} > V_{th}$, $V_{DS} > V_{DSsat}$
    - Inversion region is formed
      - V_D is high enough to counteract the V_G near the drain → "pinch-off" of the channel
      - No additional current flow is allowed





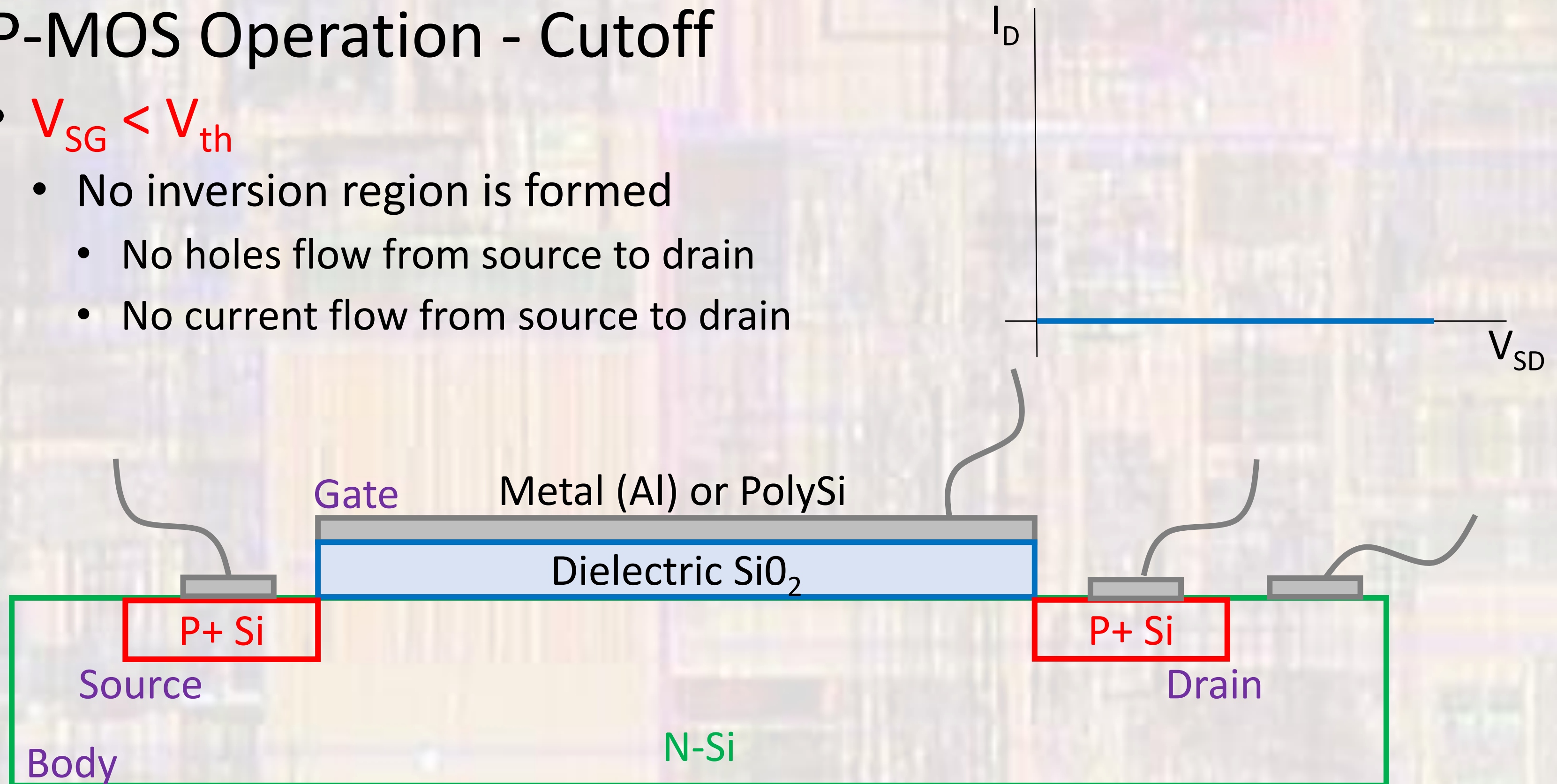
$V_{DSsat} = V_{GS} - V_{th}$

$$I_D = K_n(V_{GS} - V_{tn})^2$$

© tj

MOS I-V Characteristics

- P-MOS Operation - Cutoff
  - $V_{SG} < V_{th}$
    - No inversion region is formed
      - No holes flow from source to drain
      - No current flow from source to drain

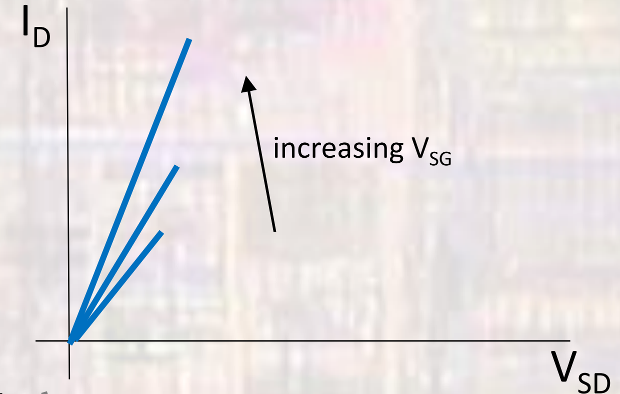


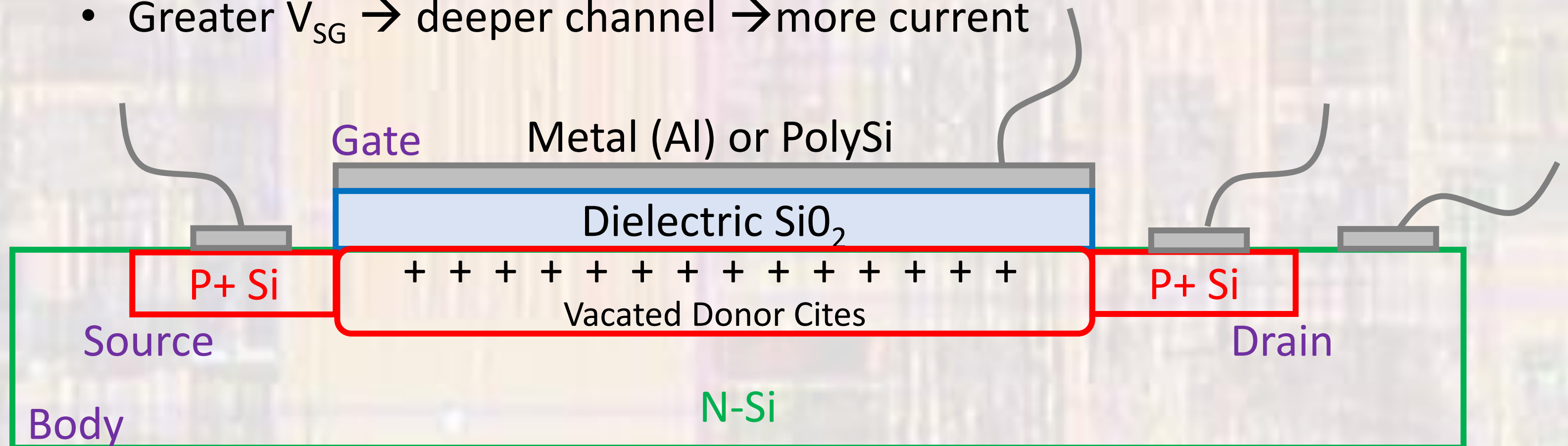
$$I_D = 0$$

© tj

MOS I-V Characteristics

- P-MOS Operation – Linear
  - $V_{SG} > V_{th}$, $V_{SD} < V_{SDsat}$
    - Inversion region is formed
      - Holes can flow from source to drain
      - Current can flow from source to drain
      - Greater V_{SG} → deeper channel → more current





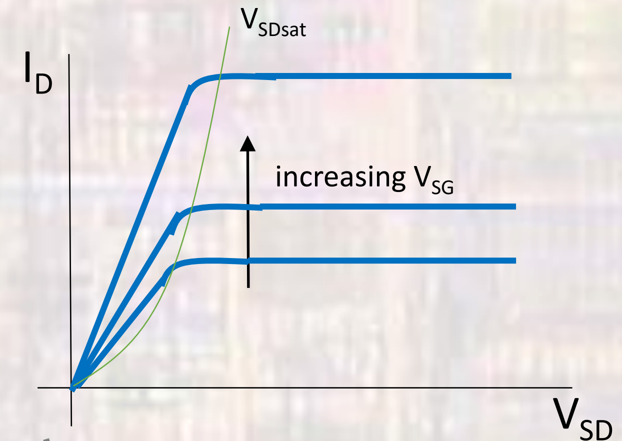
$V_{SDsat} = V_{SG} - V_{th}$

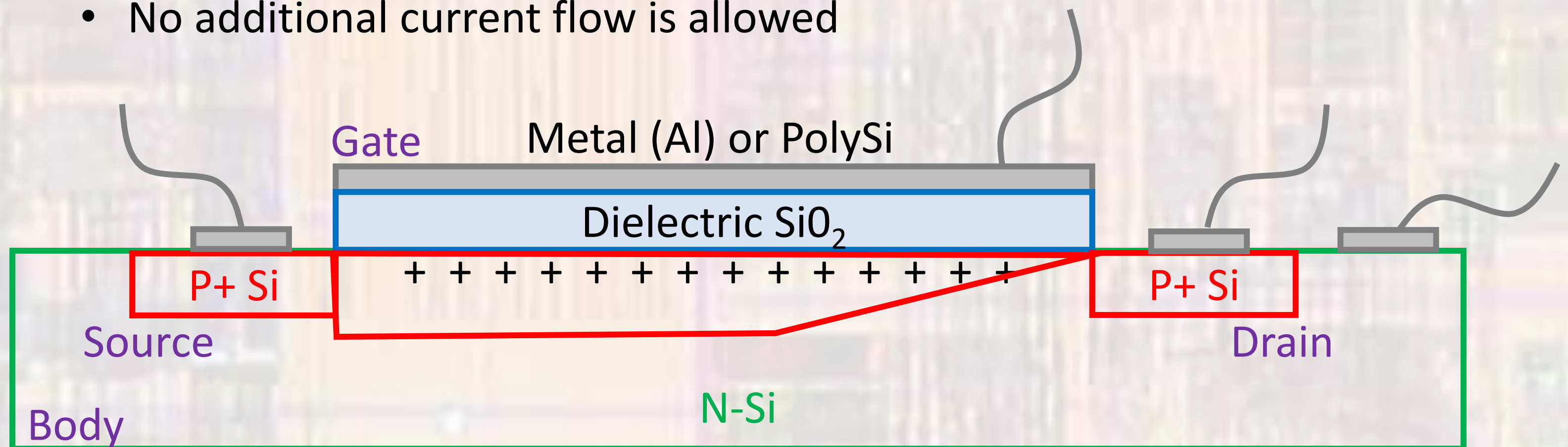
$$I_D = K_p\left[2\left(V_{SG} - V_{tp}\right)V_{SD} - V_{SD}^2\right]$$

© tj

MOS I-V Characteristics

- P-MOS Operation – Saturation
  - $V_{SG} > V_{th}$, $V_{SD} > V_{SDsat}$
    - Inversion region is formed
      - V_D is low enough to counteract the V_G near the drain → "pinch-off" of the channel
      - No additional current flow is allowed





$V_{SDsat} = V_{SG} - V_{th}$

$$I_D = K_p(V_{SG} - V_{tp})^2$$

MOS I-V Characteristics

- Parameters

$$K_n = \frac{W \mu_n C_{ox}}{2L} \qquad K_p = \frac{W \mu_p C_{ox}}{2L}$$

$$K_n = \frac{k'_n}{2}\frac{W}{L} \qquad K_p = \frac{k'_p}{2}\frac{W}{L}$$

$$k'_n = \mu_n C_{ox} \qquad k'_p = \mu_p C_{ox}$$

μ_n, μ_n, C_{ox} fixed for a given semiconductor process →

k'$_n$, k'$_p$ fixed for a given semiconductor process

Linear

$$I_D = K_n[2(V_{GS} - V_{tn})V_{DS} - V_{DS}^2] \qquad I_D = K_p[2(V_{SG} - V_{tp})V_{SD} - V_{SD}^2]$$

$$I_D = \frac{k'_n}{2}\frac{W}{L}[2(V_{GS} - V_{tn})V_{DS} - V_{DS}^2] \qquad I_D = \frac{k'_p}{2}\frac{W}{L}[2(V_{SG} - V_{tp})V_{SD} - V_{SD}^2]$$

Saturation

$V_{DS} > V_{DSsat}$ $\quad V_{DSsat} = V_{GS} - V_{th}$ $\qquad V_{SDsat} = V_{SG} - V_{th}$ $\quad V_{SD} > V_{SDsat}$

$$I_D = K_n(V_{GS} - V_{tn})^2 \qquad I_D = K_p(V_{SG} - V_{tp})^2$$

$$I_D = \frac{k'_n}{2}\frac{W}{L}(V_{GS} - V_{tn})^2 \qquad I_D = \frac{k'_p}{2}\frac{W}{L}(V_{SG} - V_{tp})^2$$

© tj

MOS Gate Capacitance

- Parameters
  - W – Transistor Width
  - L – Transistor length (channel length)
  - t_{ox} – thickness of the oxide
    - 15-20 Angstroms – 3 to 4 atom layers
    - $1.5 – 2.0\text{x}10^{-9}$ m
  - ε_0 – permittivity (dielectric constant) of free space
    - $8.85\text{x}10^{-12}$F/m
  - $\varepsilon_r(SiO_2)$ – relative permittivity multiplier for SiO_2
    - 3.9

$$C_G = W \times L \times C_{ox} = W \times L \times {}^{\varepsilon_{ox}}/_{t_{ox}} = W \times L \times {}^{\varepsilon_0 \varepsilon_r}/_{t_{ox}}$$

$$C_{Gn} = W \times L \times {}^{k'_n}/_{\mu_n} \qquad C_{Gp} = W \times L \times {}^{k'_p}/_{\mu_p}$$

© tj