# Parallel Communications APB

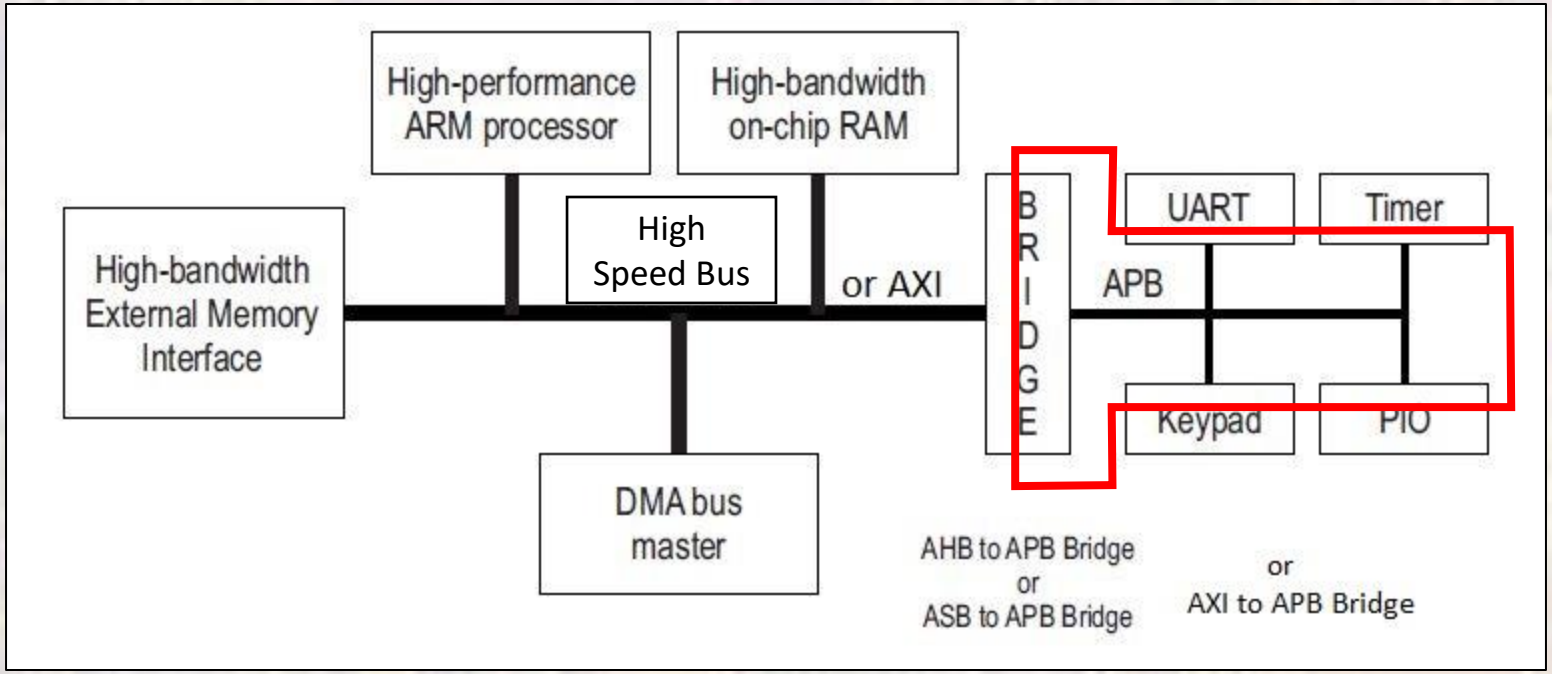
Last updated 2/15/24

# Parallel Communications - APB

- ARM
  - By far the most widely accepted architecture
  - AMBA – Advanced Microprocessor Bus Architecture
    - CHI - Coherent Hub Interface - The highest performance, used in networks and servers
    - ACE - AXI Coherency Extensions - Used in big.LITTLE™ systems for smartphones, tablets, etc.
    - AXI - Advanced eXtensible Interface - The most widespread AMBA interface. Connectivity up to 100's of Masters and Slaves in complex SoC's
    - AHB - Advanced High-Performance Bus - The main system bus in microcontroller usage
    - APB - Advanced Peripheral Bus - Minimal gate count for peripherals
    - ATB - Advanced Trace Bus - For moving trace data around the chip

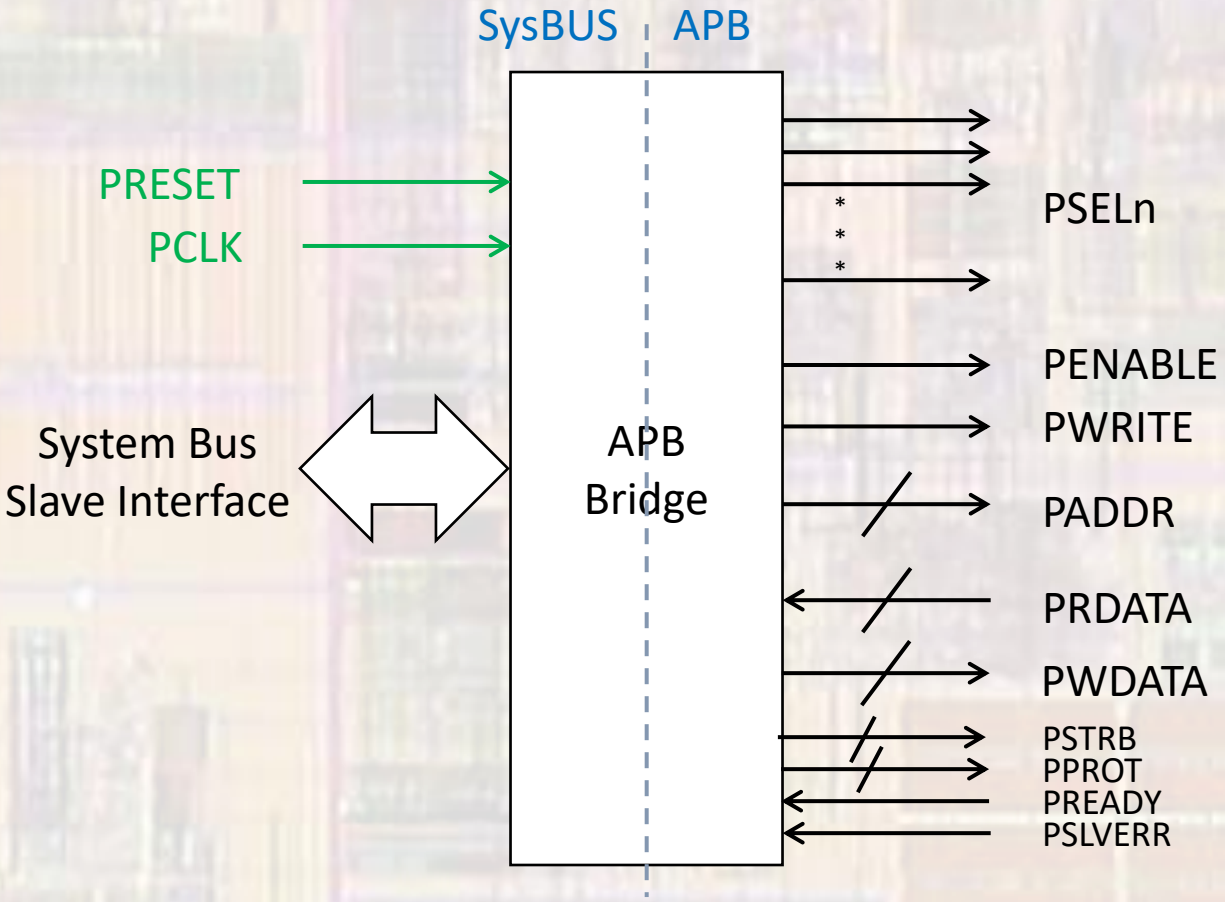
# Parallel Communications - APB

- ARM - APB
  - Advanced Peripheral Bus



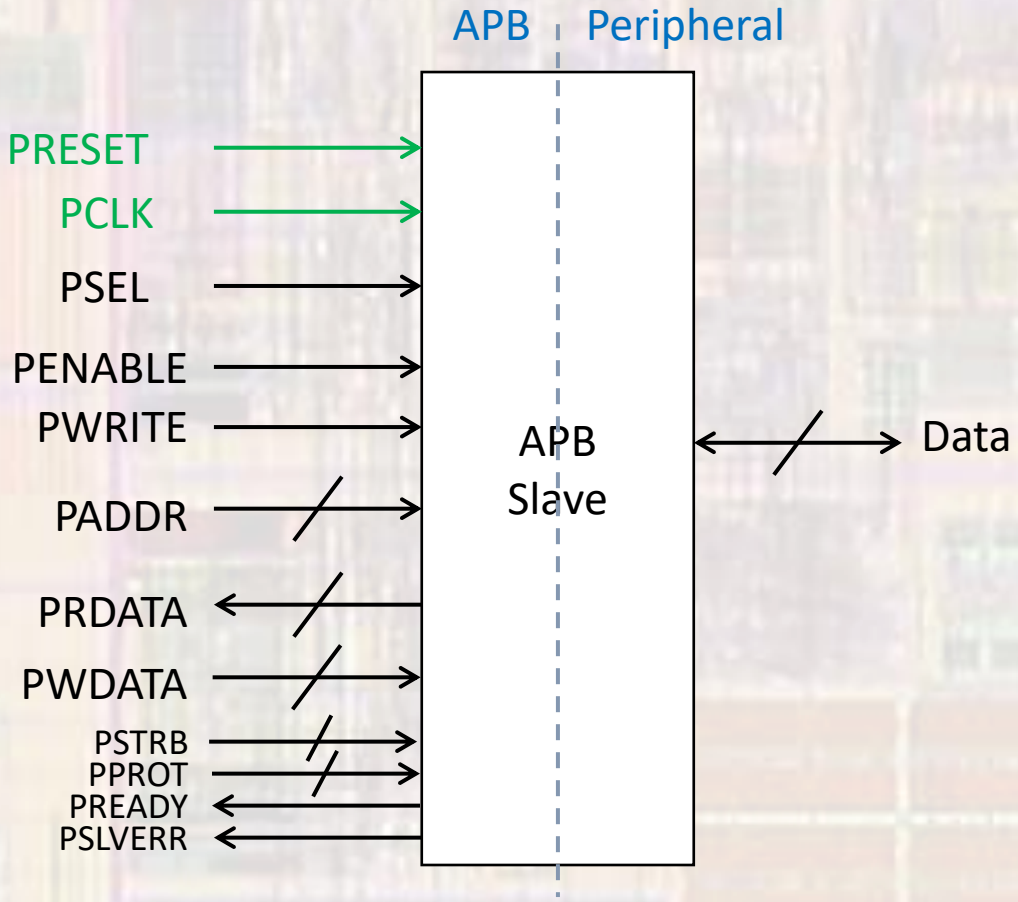
# Parallel Communications - APB

- APB System Bridge
  - Connects the system bus to the APB



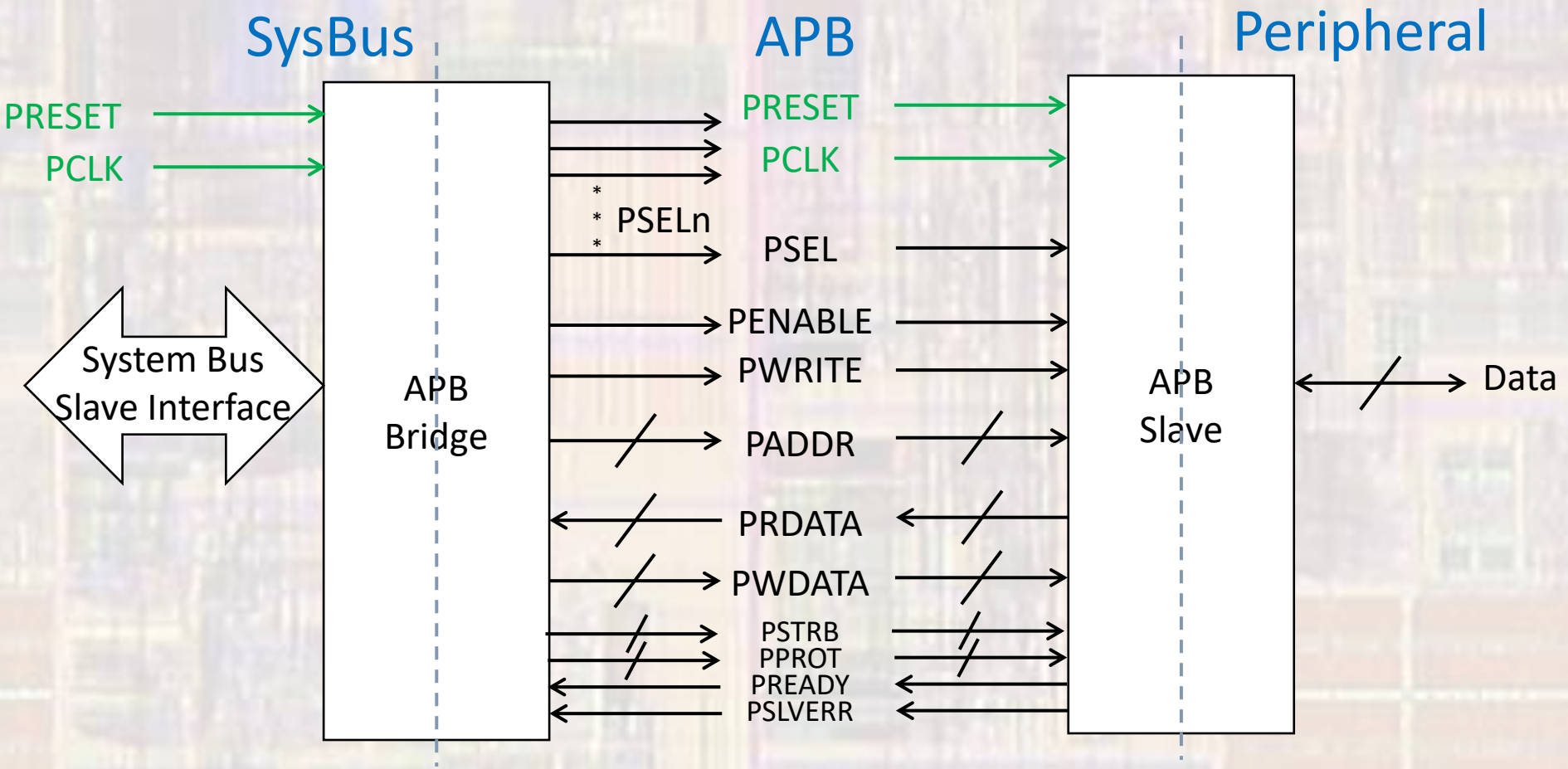
# Parallel Communications - APB

- APB Slave
  - Integrated into each peripheral tied to the APB



# Parallel Communications - APB

- APB Connections



# Parallel Communications - APB

- APB Signals
  - PCLK – Derived system clock – gated, frequency
  - PRESET – Derived system reset
  - PADDR – Memory mapped address – up to 32 bits
  - PSELx – Peripheral select
  - PENABLE – Used for signaling
  - PWRITE – Write signal
  - PWDATA – Data to Write to the peripheral – up to 32 bits
  - PRDATA – Data to Read from the peripheral – up to 32 bits

  - PREADY – Allows peripherals to extend a data transfer
  - PSTRB – Used to select a byte to update on a write (2 bits)
  - PSLVERR – Indicates the slave detected an error
  - PPROT – Indicates transaction type: Regular, Privileged, Secure (2 bits)

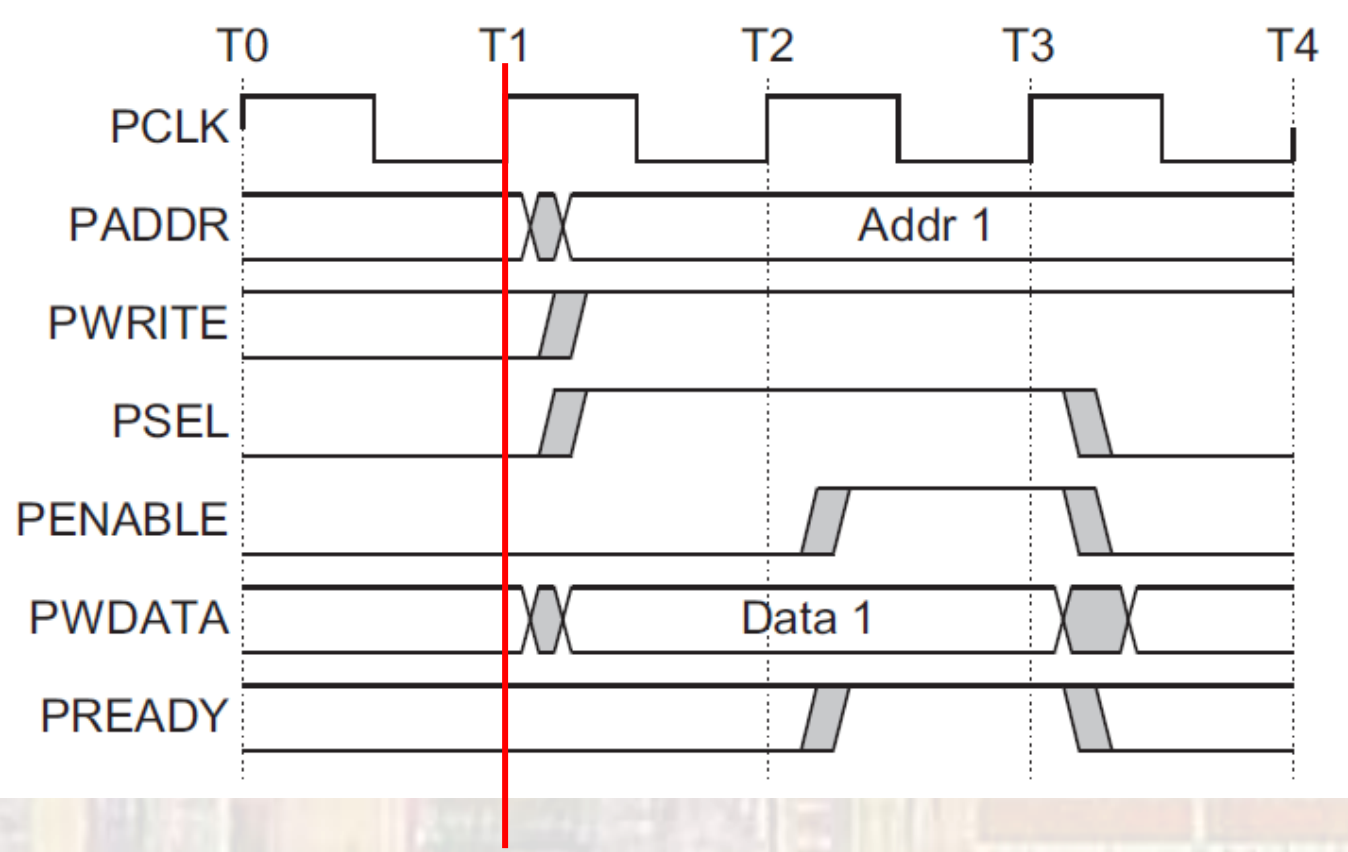
# Parallel Communications - APB

- APB Write

SETUP

@T1

Bridge
→ Address
→ Write
→ Select
→ Data



# Parallel Communications - APB

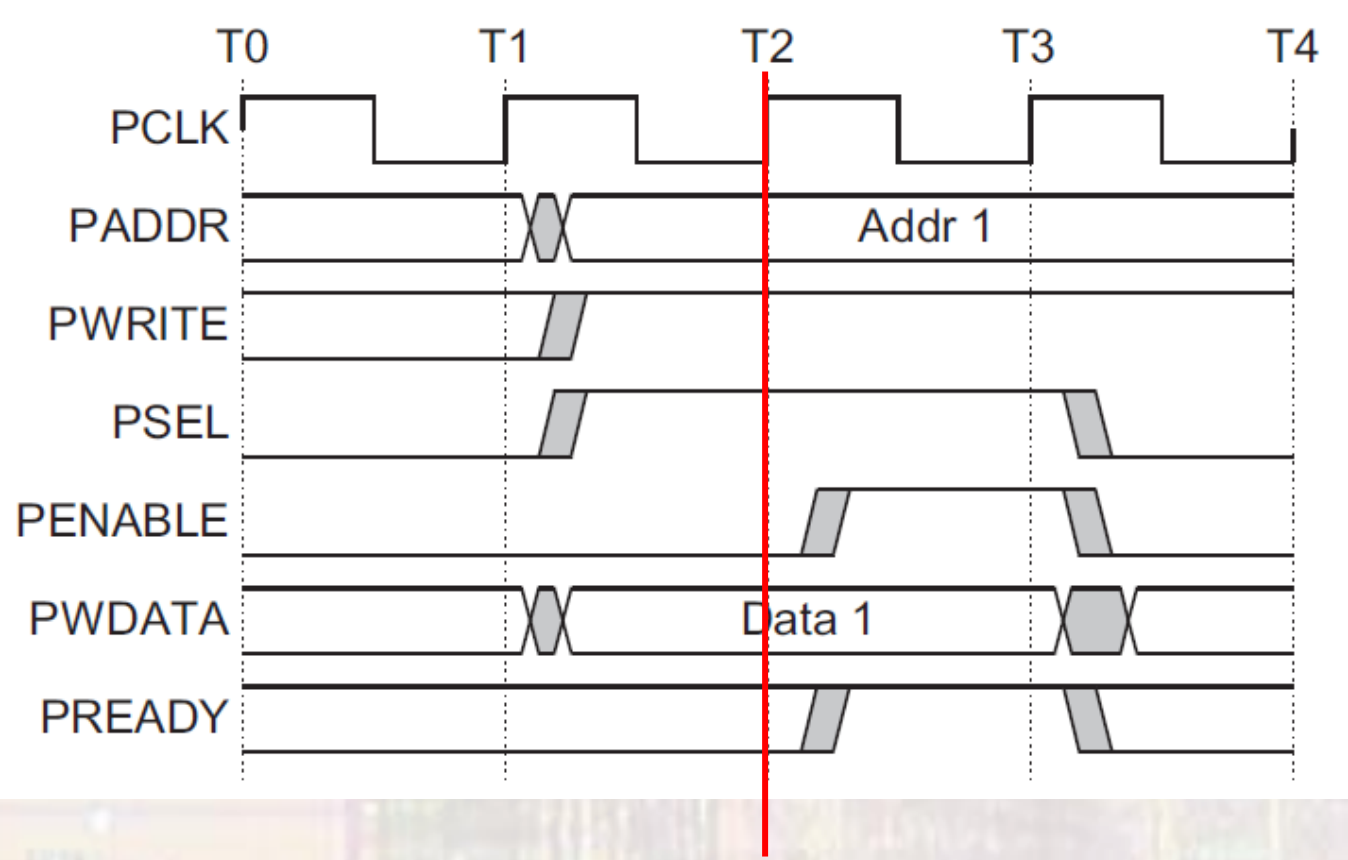
- APB Write

ACCESS

@T2

Bridge
→ ENABLE

Slave
→ READY



# Parallel Communications - APB

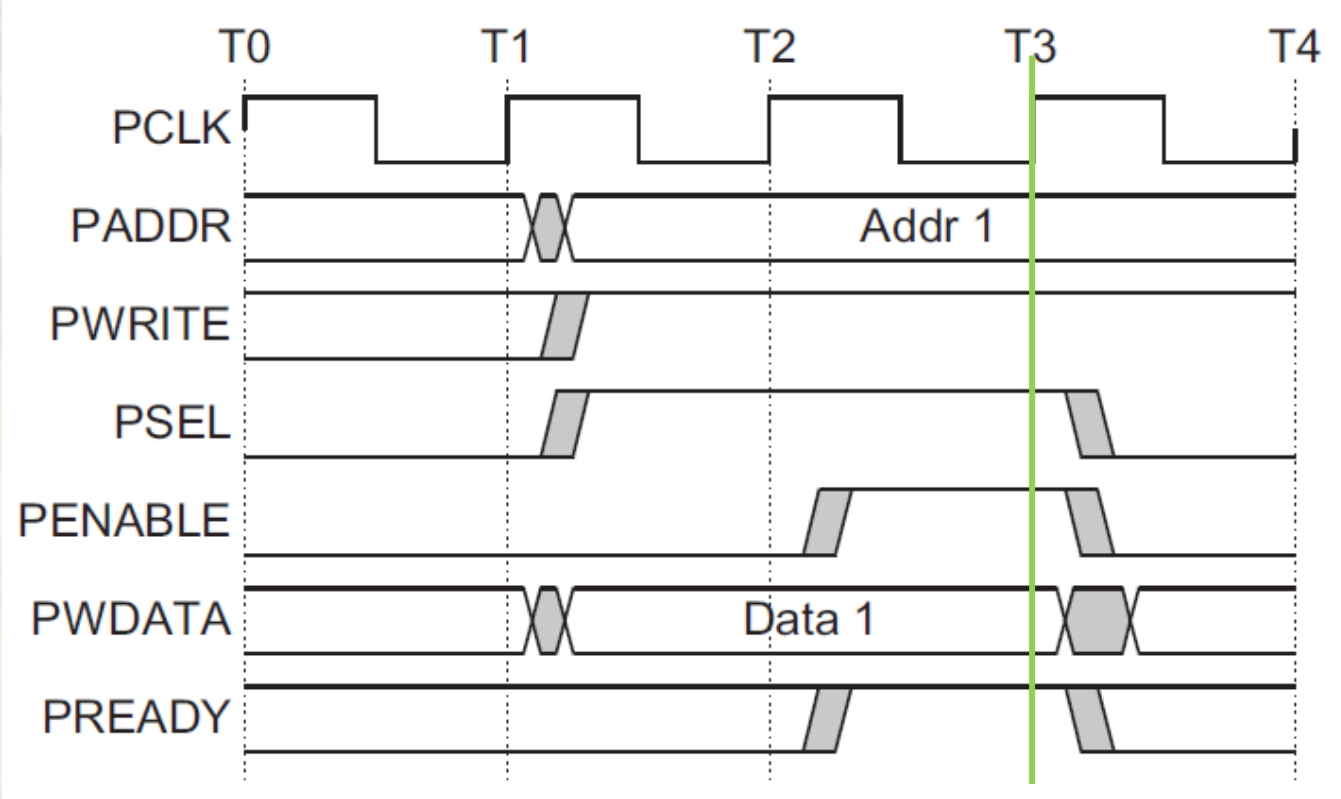
- APB Write

@T3 (1 clk after READY goes ↑)

Slave has captured the data

Bridge → ENABLE low

Slave → READY low

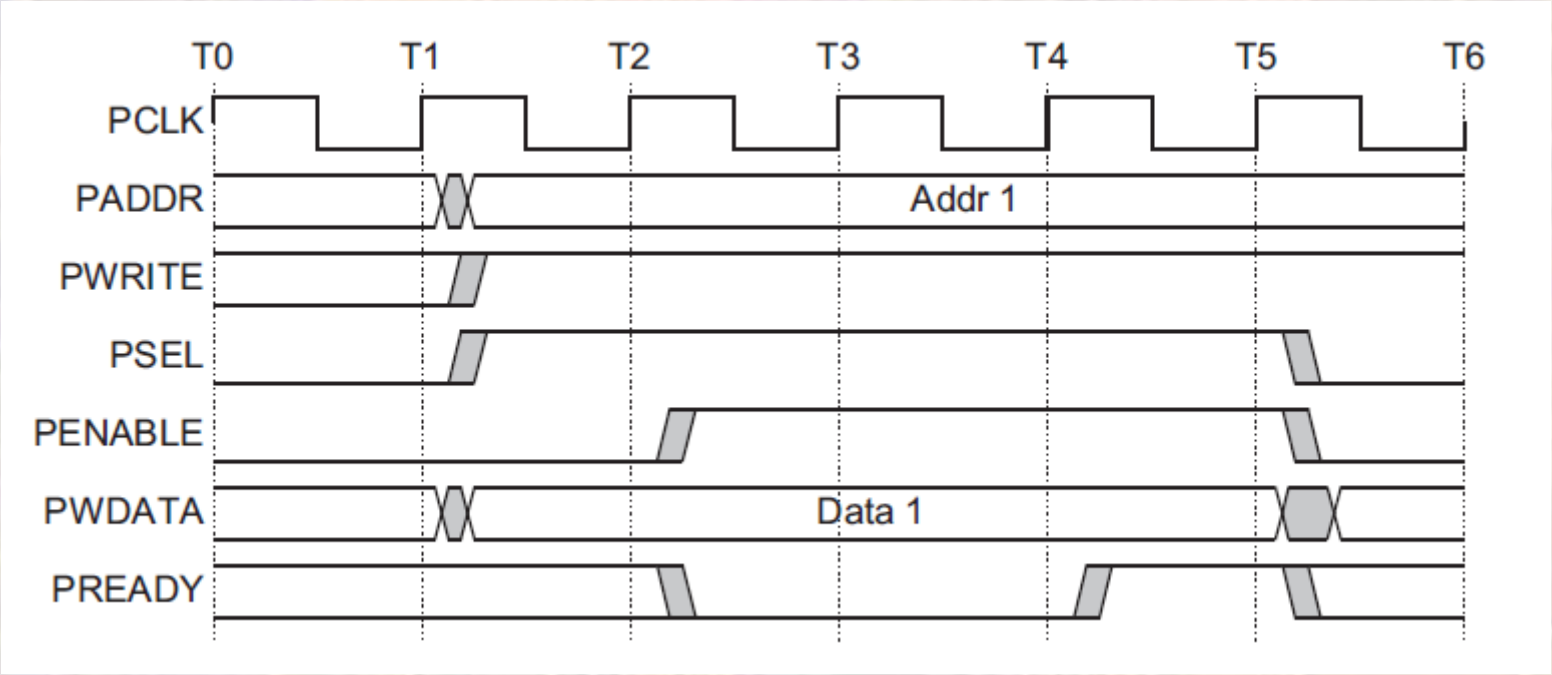



All APB transactions are at least 2 cycles long
- 1st clock after READY goes high

ADDR, WRITE, SEL and DATA must be stable through T3

# Parallel Communications - APB

- APB - Extended Write
  - Slave uses READY signal to delay the completion of the write



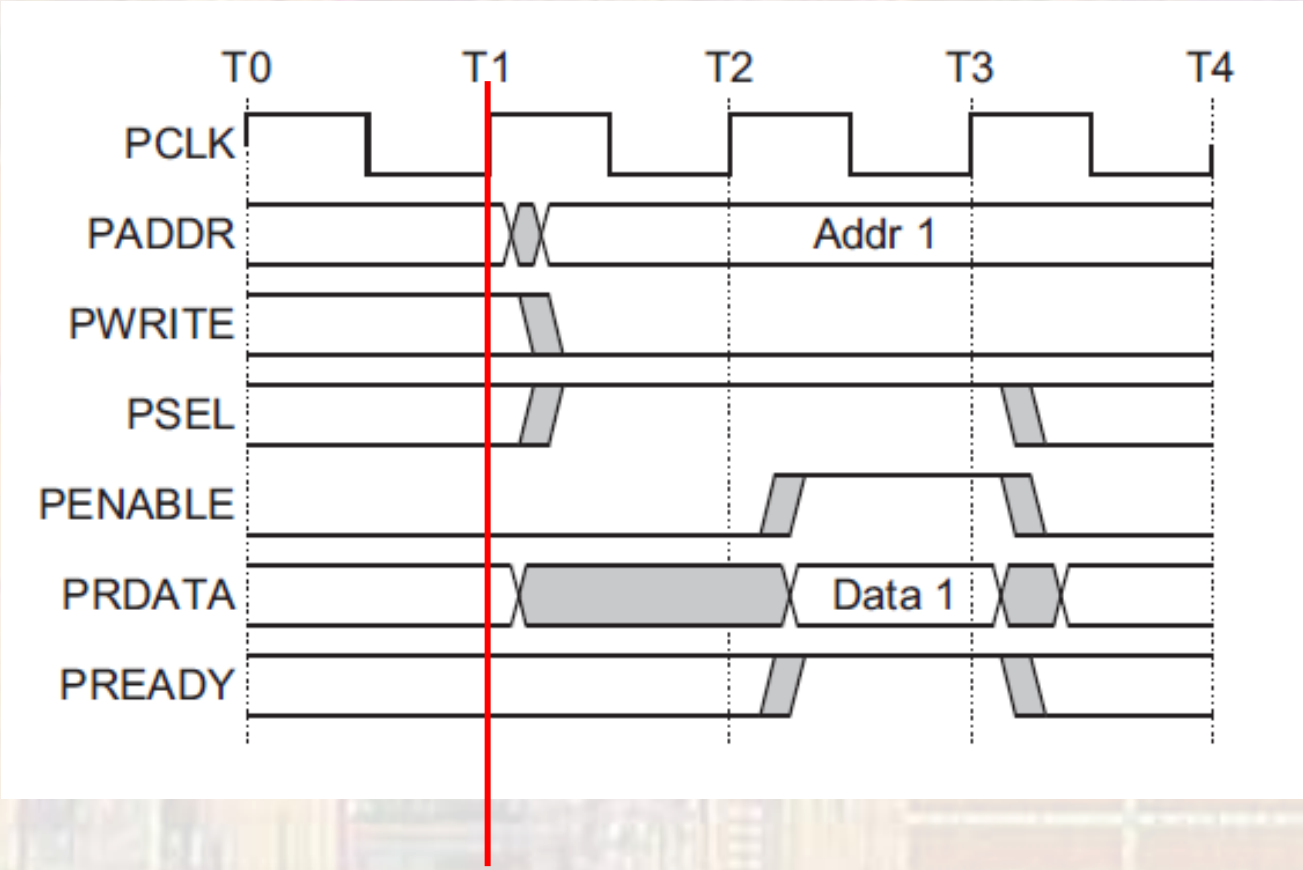
# Parallel Communications - APB

- APB - Read

SETUP

@T1

Bridge
→ Address
→ Write
→ Select



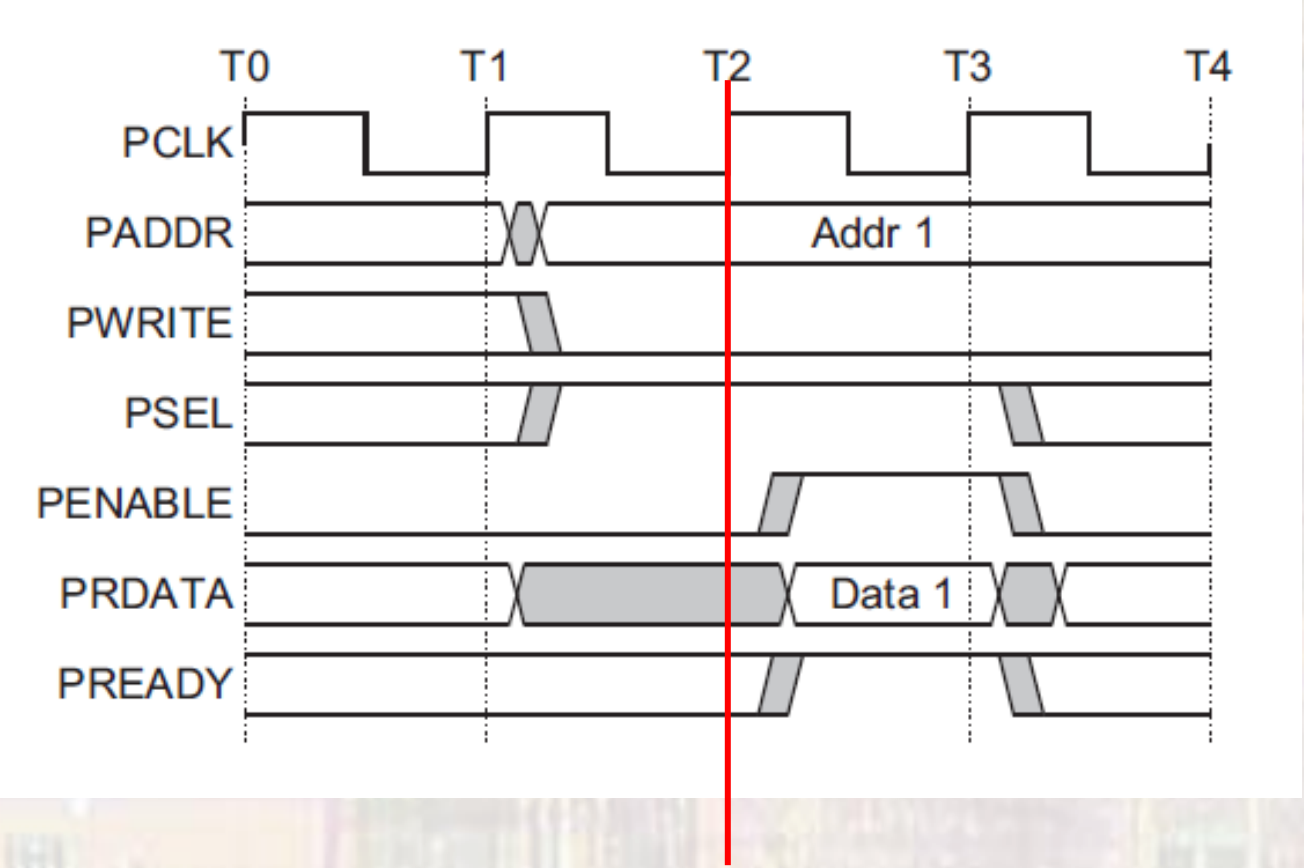
# Parallel Communications - APB

- APB - Read

ACCESS

@T2

Bridge
→ ENABLE
Slave
→ READY
→ Data



# Parallel Communications - APB

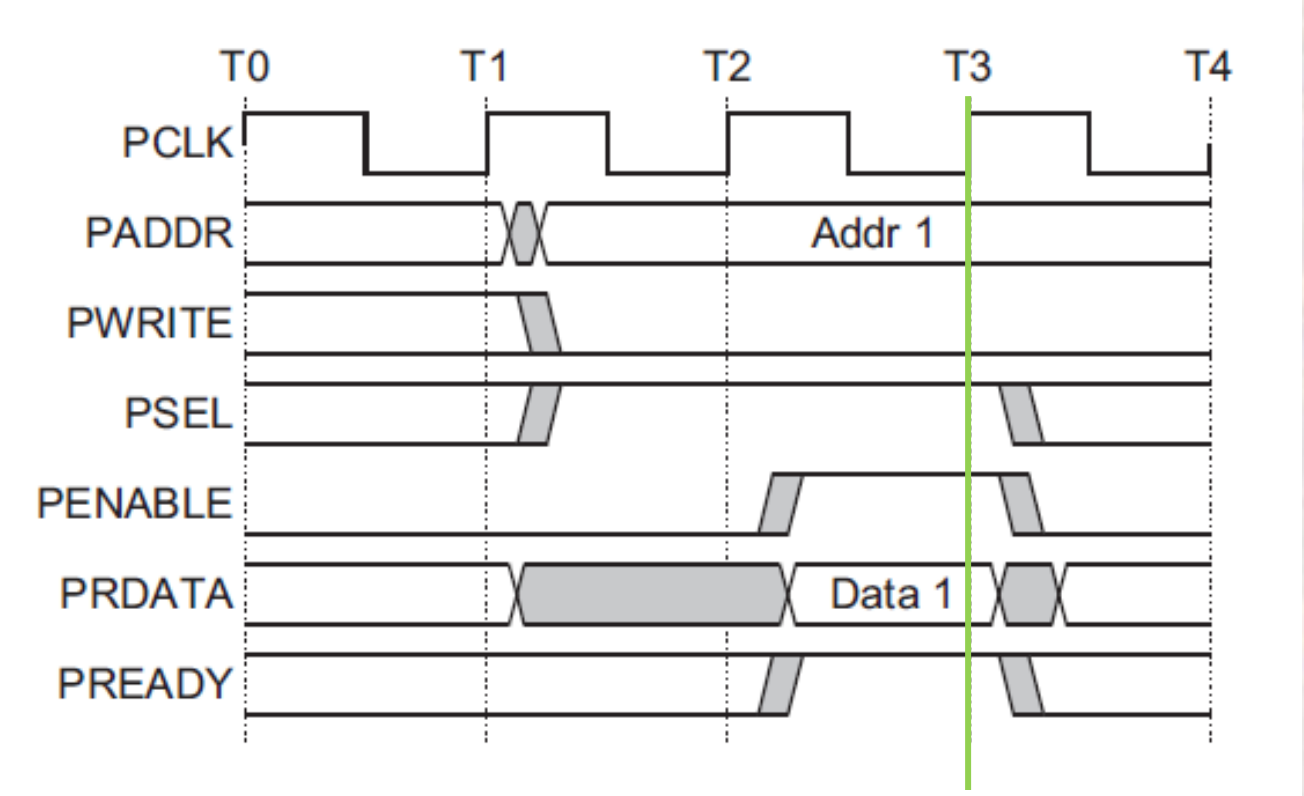
- APB - Read

@T3 (1 clk after READY goes ↑)

Bridge has captured the data

Bridge → ENABLE low

Slave → READY low

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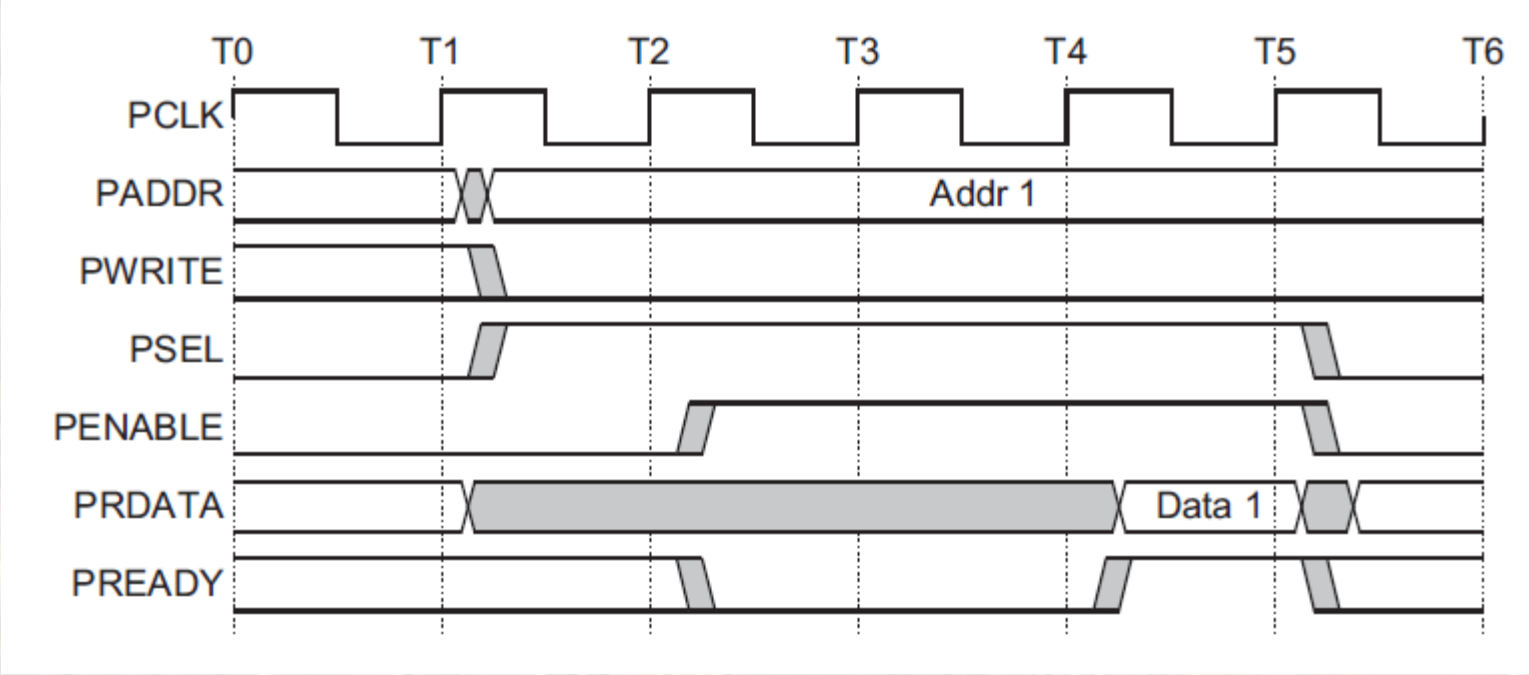
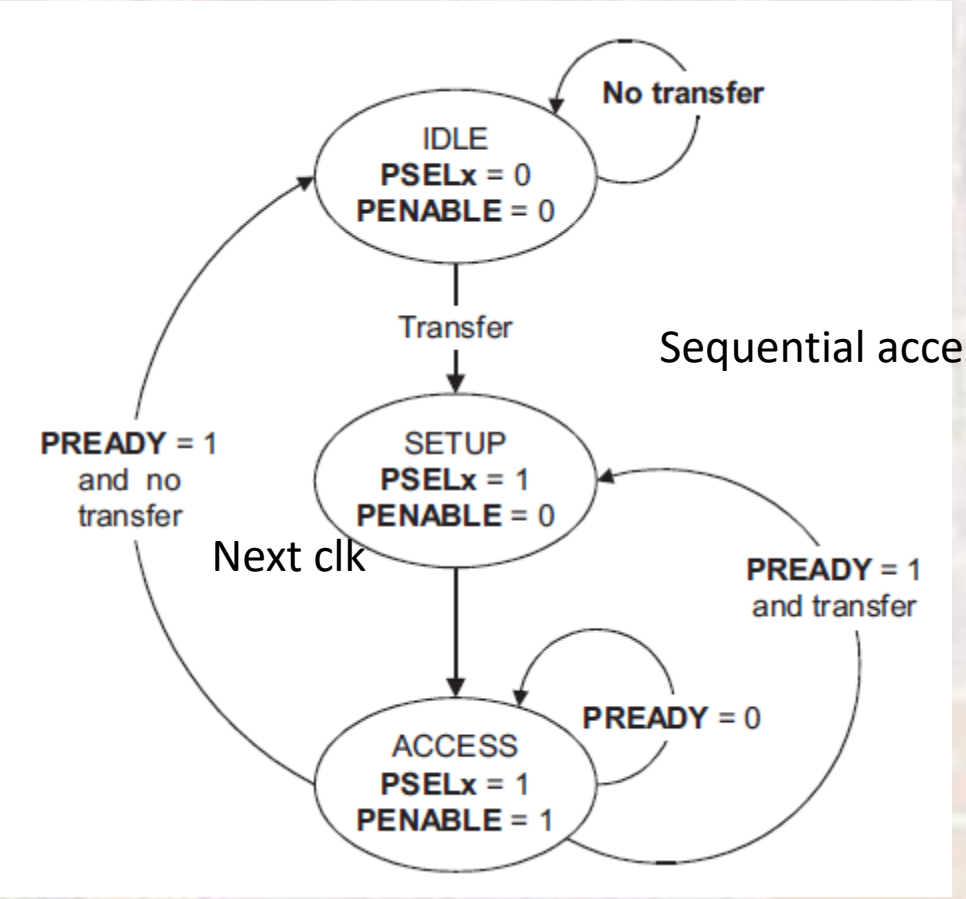


# Parallel Communications - APB

- APB - State Diagram



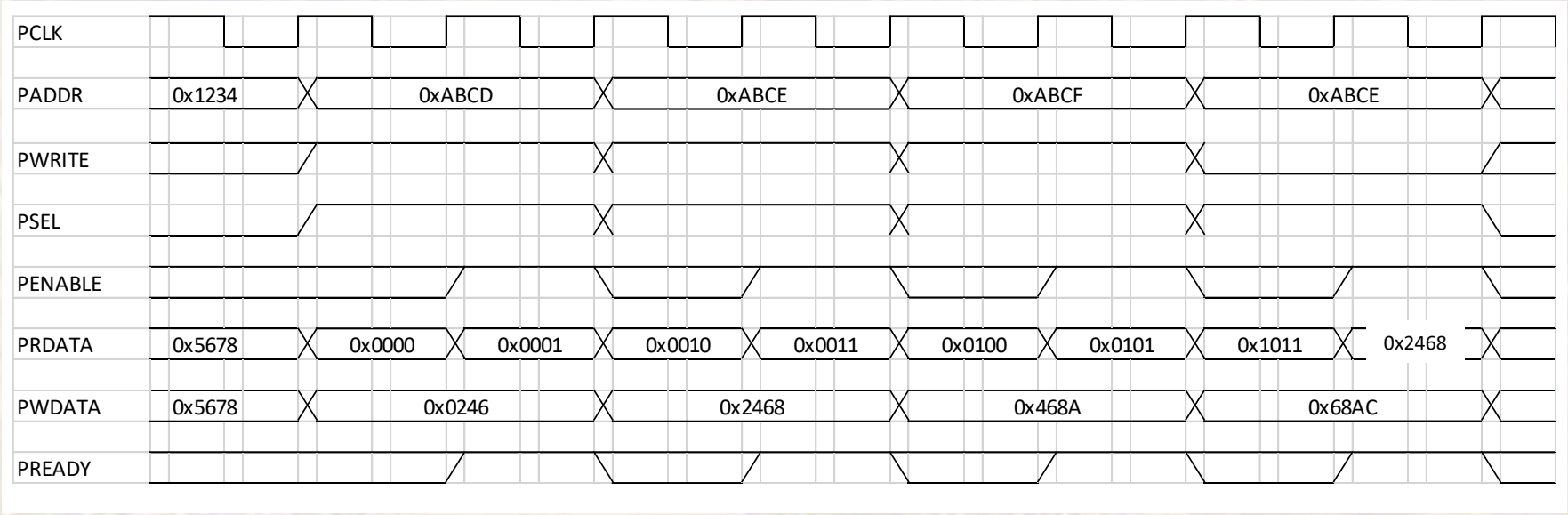

 

# Parallel Communications - APB

- AMBA - APB
  - Special Note
    - Even though the APB has separate Read and Write Data paths it is not capable of full duplex operation.
    - Why ?

# Parallel Communications - APB

- APB - Example



# Parallel Communications - APB

- APB - Example