

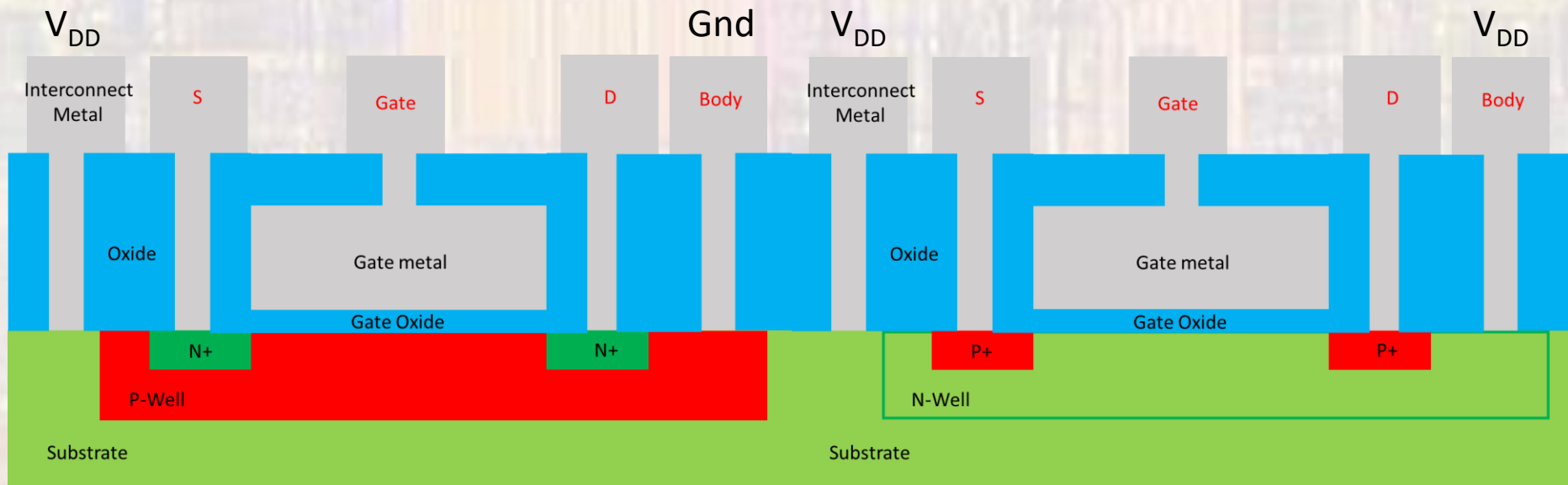
# Planer CMOS Processing

Last updated 1/18/23

A faded, light-colored image of a CMOS chip layout is visible in the background of the lower half of the slide. It shows a complex grid of lines and rectangular blocks, representing the intricate circuitry of a microchip.

# Planer CMOS Processing

- Digital Planer CMOS Structure
  - Dominant until about 2015
  - Still used for older technologies
  - Still used for analog technologies



# Planer CMOS Processing

- Implant a P-well into an N-Wafer

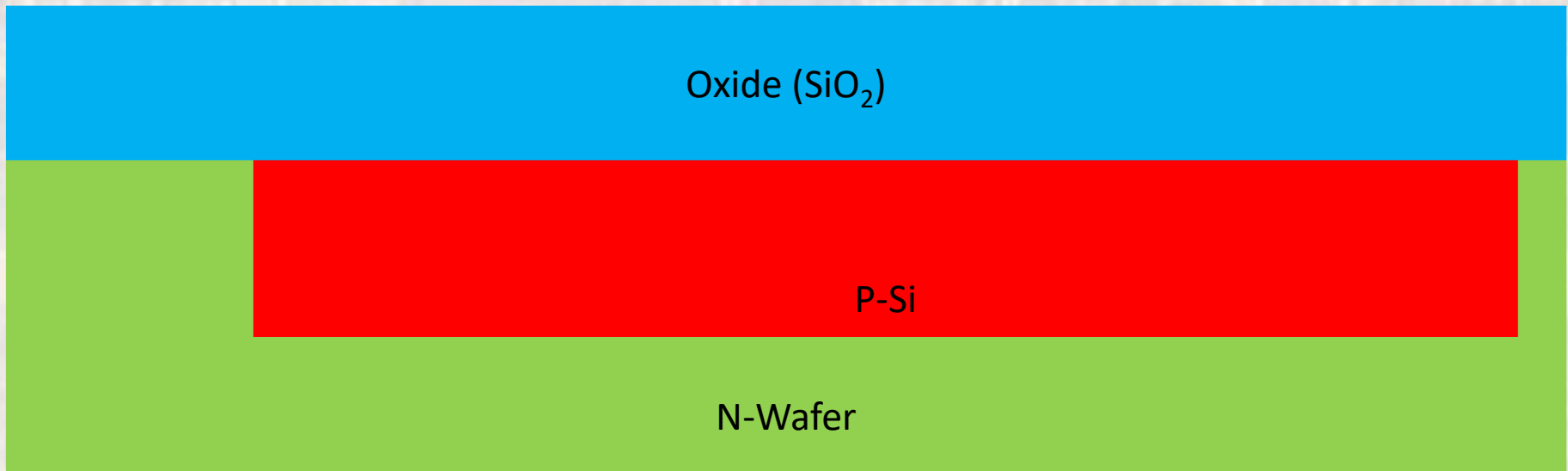
N-Channel



# Planer CMOS Processing

- Deposit thick oxide

N-Channel



# Planer CMOS Processing

- Etch oxide for the “Active area”
  - Source + drain + gate

N-Channel



# Planer CMOS Processing

- Grow the thin gate oxide

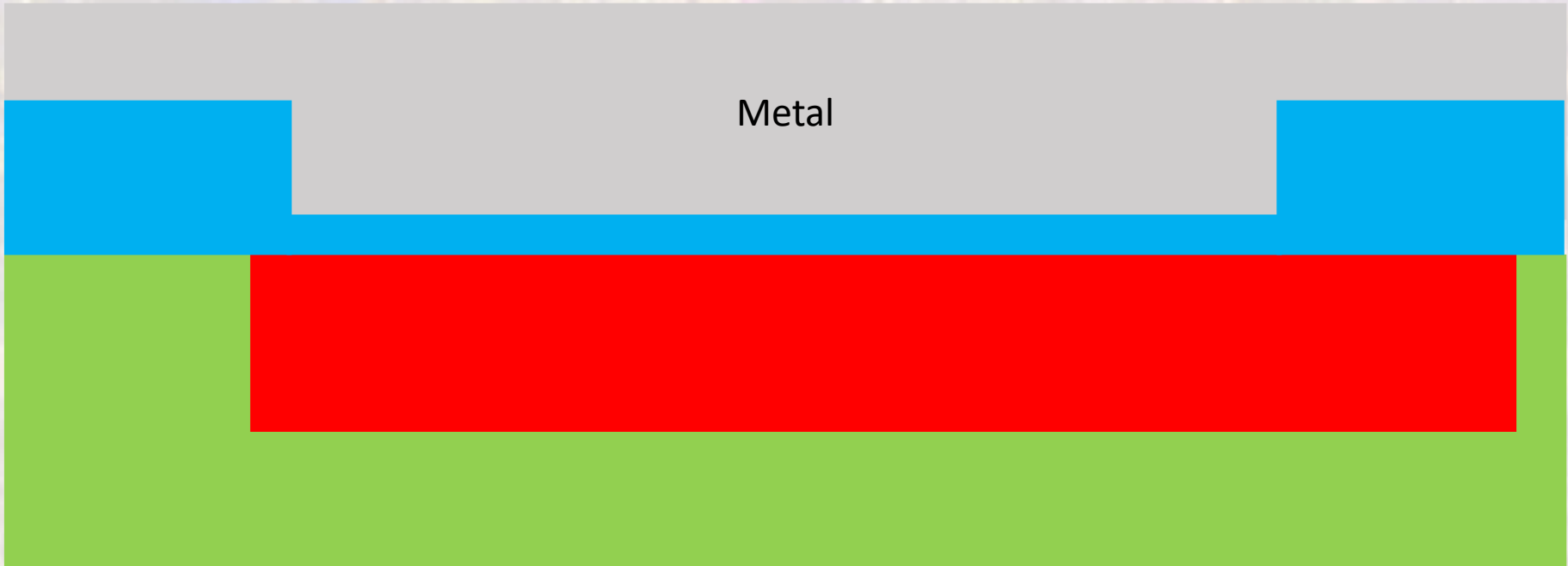
N-Channel



# Planer CMOS Processing

- Deposit gate metal
  - Aluminum or Poly-Silicon

N-Channel



# Planer CMOS Processing

- Pattern and etch the gate metal

N-Channel





# Planer CMOS Processing

- Implant Phosphorus (N+)
  - N+ regions form where only thin oxide is present

N-Channel



# Planer CMOS Processing

- Deposit more oxide

N-Channel



# Planer CMOS Processing

- Pattern and etch for contacts

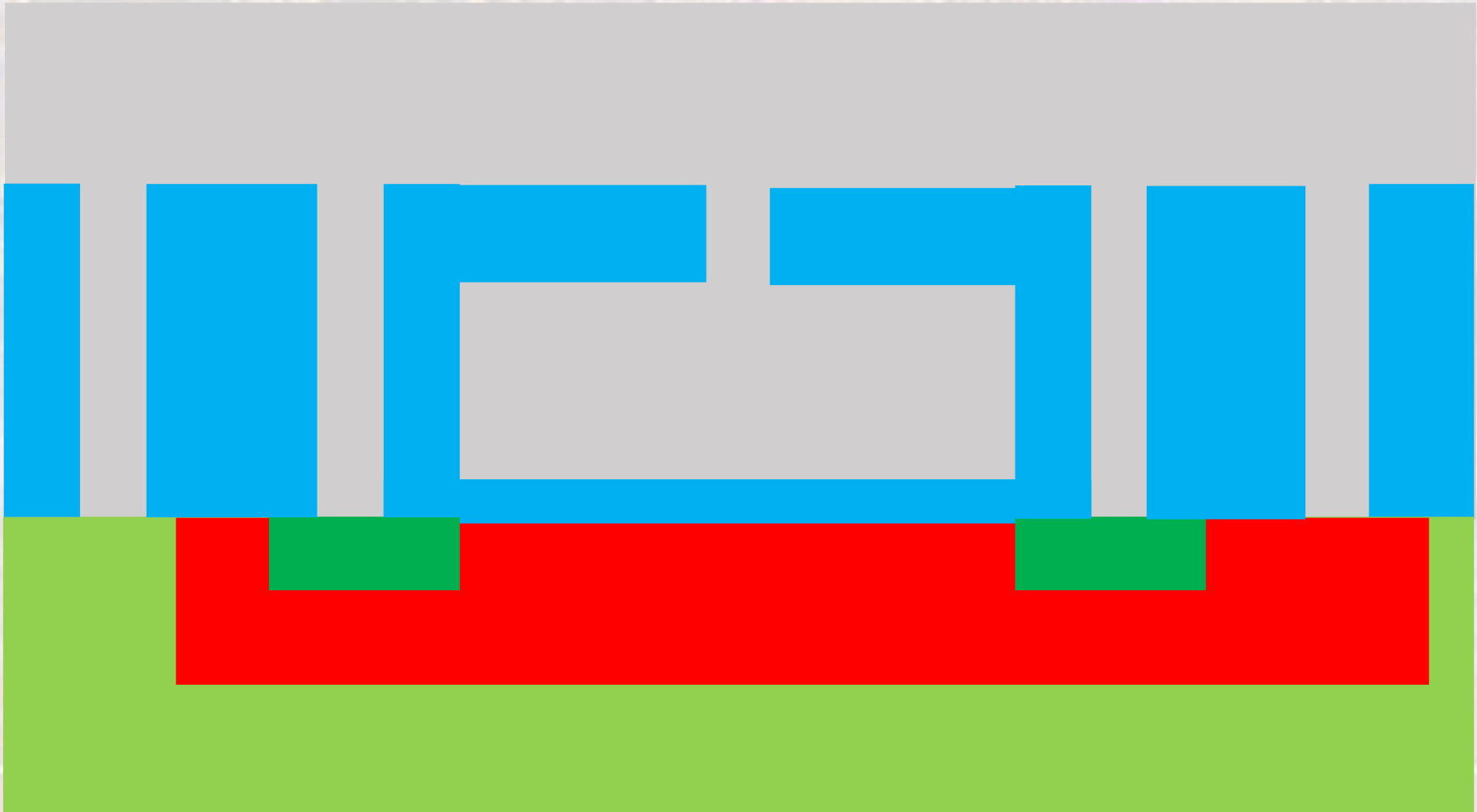
N-Channel



# Planer CMOS Processing

- Deposit interconnect metal

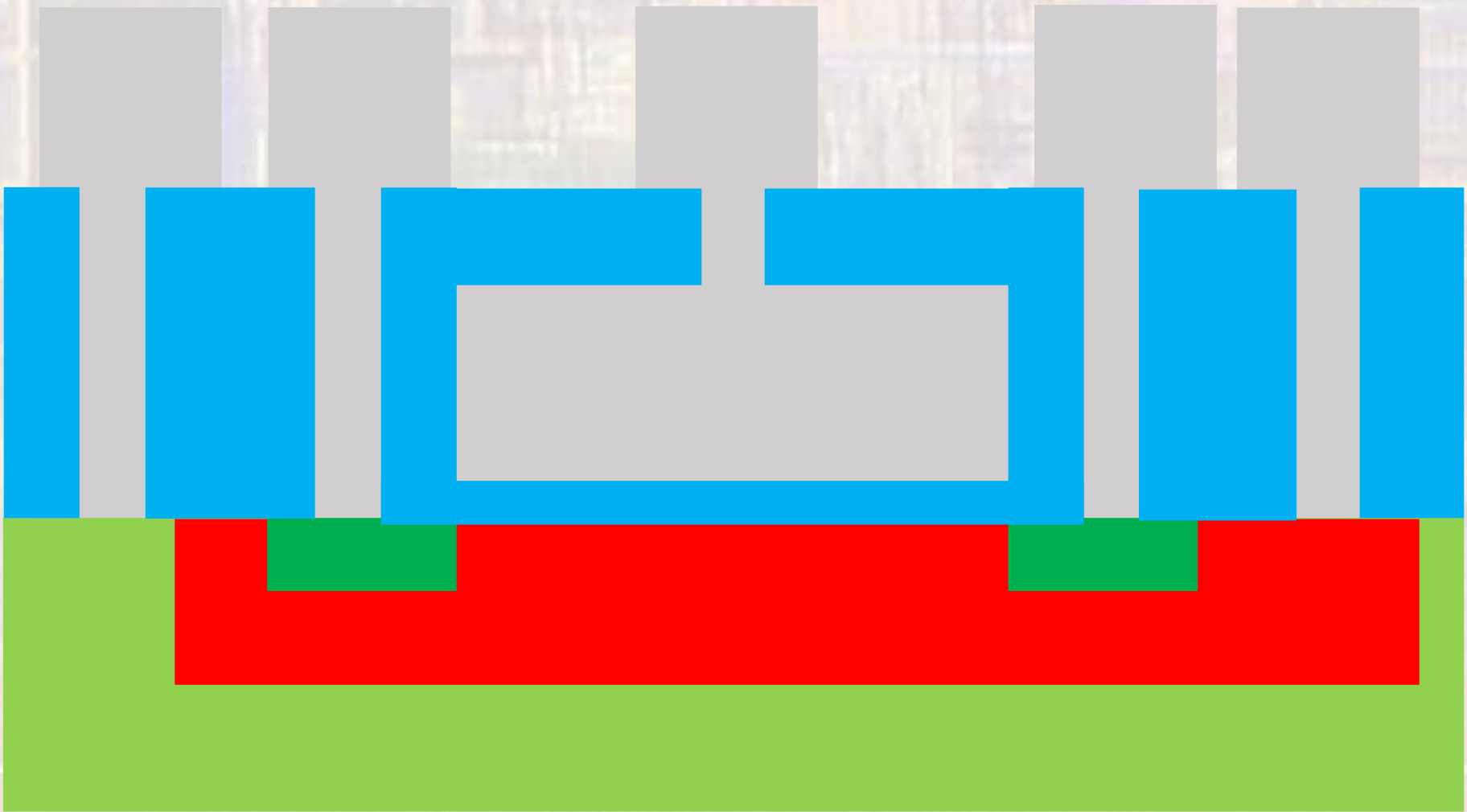
N-Channel



# Planer CMOS Processing

- Etch interconnect metal

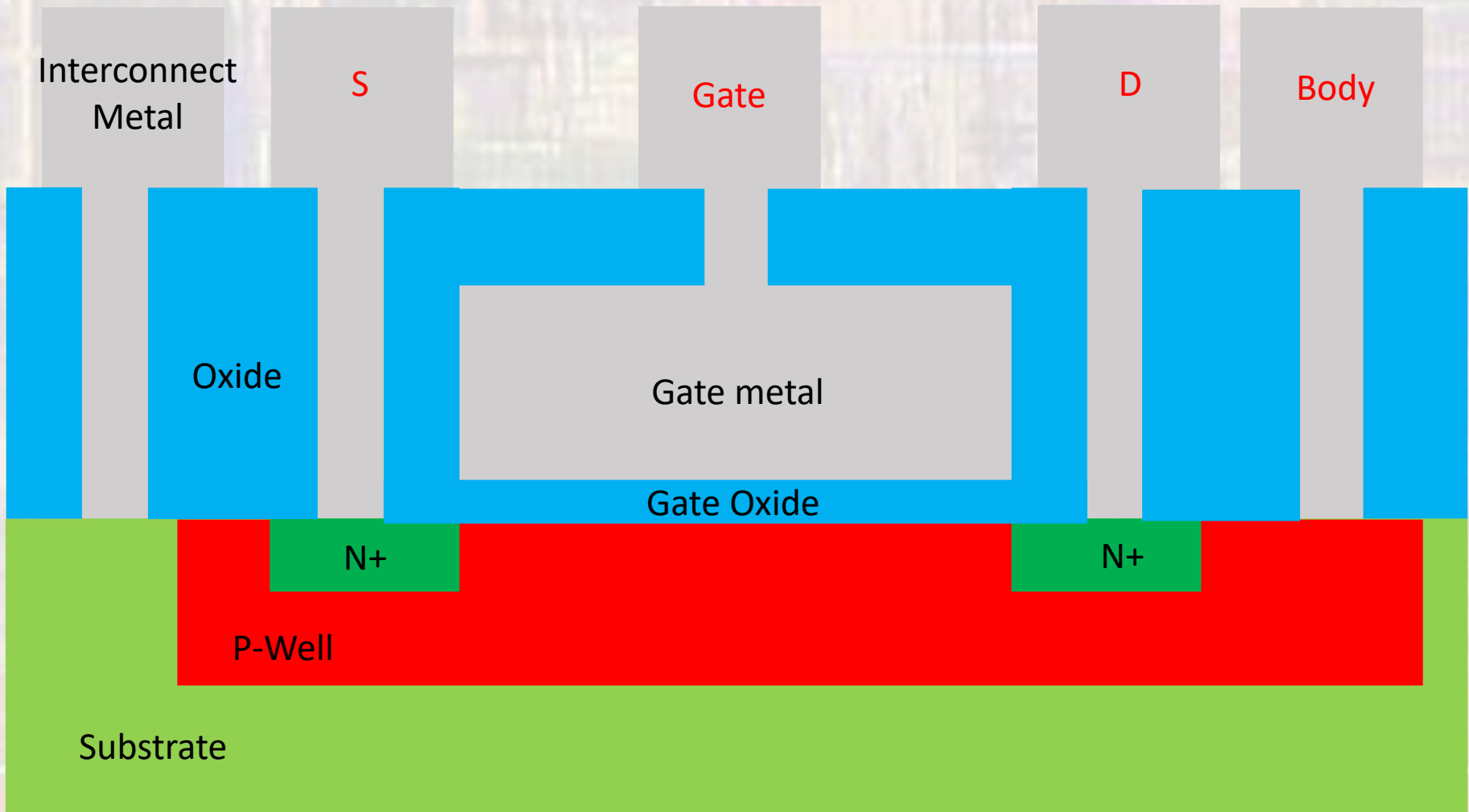
N-Channel



# Planer CMOS Processing

- Final N-Channel

N-Channel



# Planer CMOS Processing

- Final P-Channel

