# ELE 455/555

Spring 2016

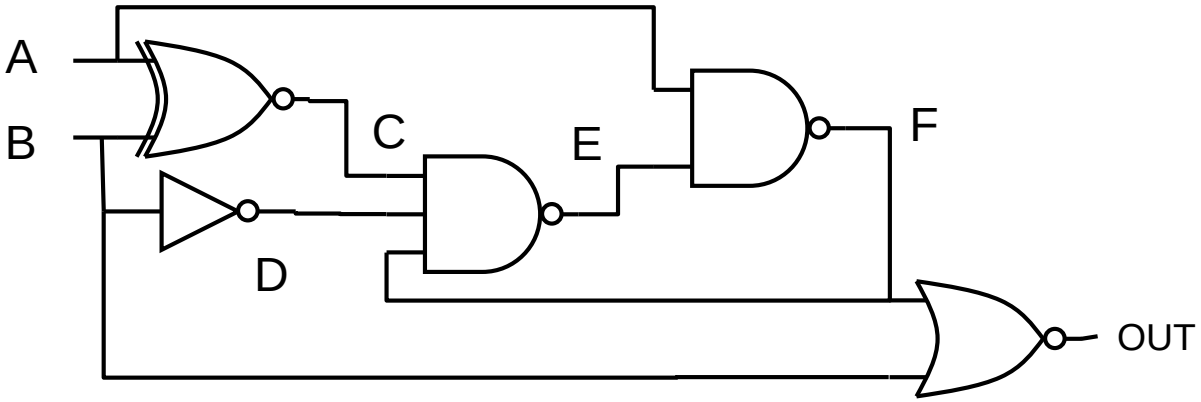
# Homework 1A

Due 1/26

Beginning of Class

A1 – create a full truth table for the following circuit – 10pts

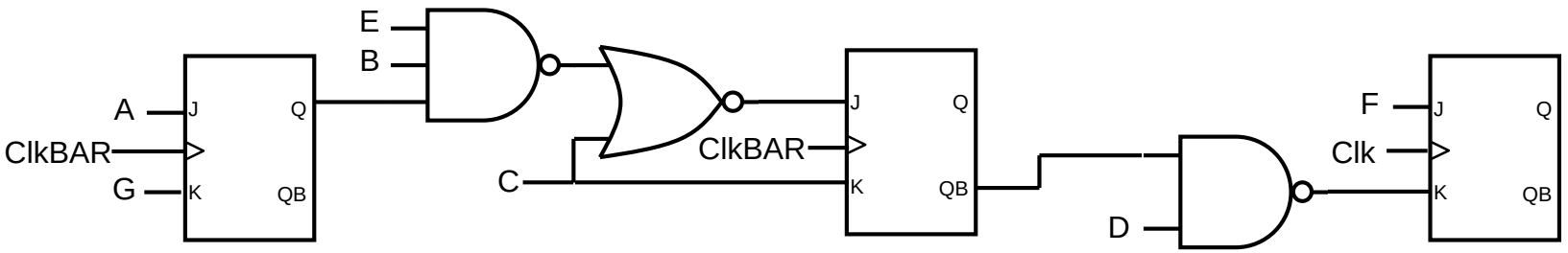
(be sure to include all intermediate nodes)



A2 – Assuming the gates have the characteristics identified below –
what is the fastest acceptable clock frequency– 10pts

show your work

| | |
|---|---|
| **J/K - T clock to Q/Qbar** | **50ps** |
| **J/K - T setup** | **10ps** |
| **J/K - T hold** | **10ps** |
| **T - In to out (sequential logic)** | **20ps** |
| **Signals A-G arrive syncronously** | |



A3 - Write 43.673 using standard floating point notation AND determine the error associated with this representation.

you must show your work – 10pts

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
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