ELE 455/555

Spring 2016

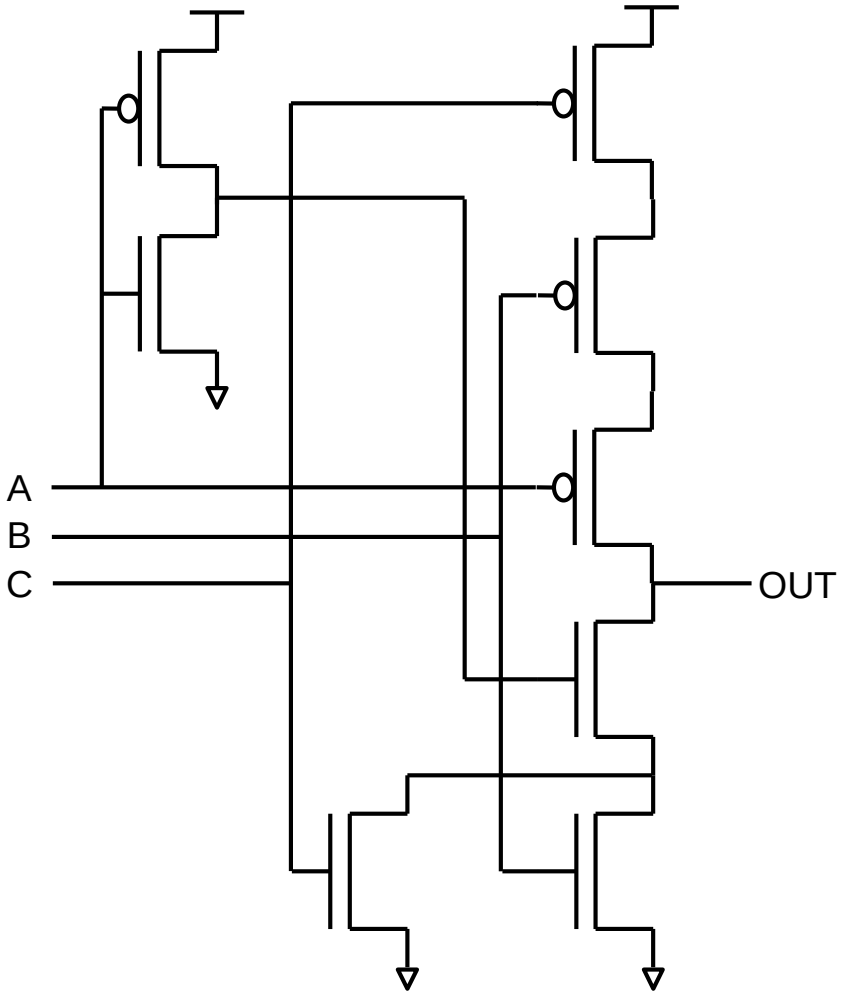
Homework 2

Due 2/2

Beginning of Class

1. Logic Circuits – 10pts

a) Create a truth table for the following circuit: - 7pts

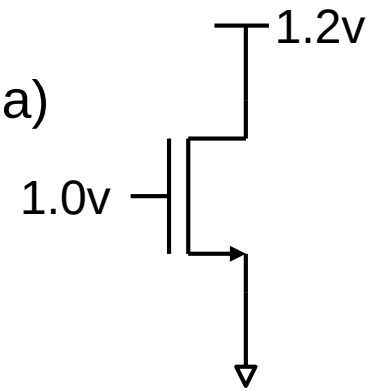


b) What is it's function? – 3pts

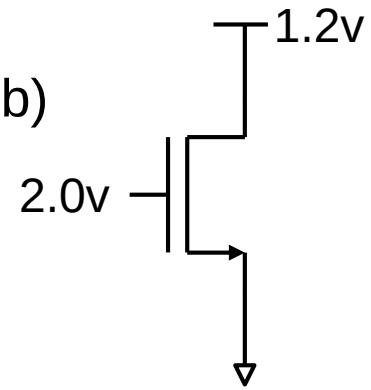
2. MOS Transistors – 10pts

Given an n-channel silicon mosfet with W=0.2μ, L=45nm, t_{ox}=40Å, μ_n=500cm^2/V-s and V_t=0.6v, determine I_{DS} for the following circuits:

a)



b)



3. Frequency – 10pts

Assuming a design optimized to match rise and fall times, how would you expect the maximum operating frequency to vary with supply voltage? (use the simplified equations from the class 3 notes - show your work)

Why do operating voltages keep dropping?

4. Power – 10pts

Processor A can execute 1 instruction per clock cycle
@2V, Processor A's max operating frequency is 200MHz
@1V, Processor A's max operating frequency is 100MHz
If you need to execute 50M instructions per second

a) Which voltage/frequency combination should you operate at to minimize active power?

b) Is there a second operating point with the same power performance? What is it?

5. Pipeline – 10pts

The 4 stages of a data path have the following latencies

Stage 1: 200ps, Stage 2: 400ps, Stage 3: 300ps, Stage 4: 100ps

Pipelining these stages adds 20% to the latency of each stage

a) Should you create a pipeline or not? (show your work)

b) At what latency penalty (%) does your decision change? (show your work)

6 – Architecture Analysis - 10pts

Identify the specific processor in your computer (or one in the laptop or lab computer

A) What is the processor

B) Draw a very simple architectural diagram including CPU and Memory Hierarchy

C) How many pipeline stages does this processor have

7 – Fill in the memory values for the Processor Z assembly code below – 10pts

start the code at memory location 0x01A1

(be sure to put the code in the proper format)

```
        ldz     R2
loop:   add     R0,R2
        dec     R1
        bnz     R1,loop2
        stz     R2
loop2:  bnz     R1,loop
        ldi     R2,12
```

ADDRESS						DATA	
Hex						Hex	
0	1	A	1				
0	1	A	2				
0	1	A	3				
0	1	A	4				
0	1	A	5				
0	1	A	6				
0	1	A	7				
0	1	A	8				
0	1	A	9				
0	1	A	A				

8 – Reverse assemble the Processor Z code below – 10pts

(be sure to put the code in the proper format)

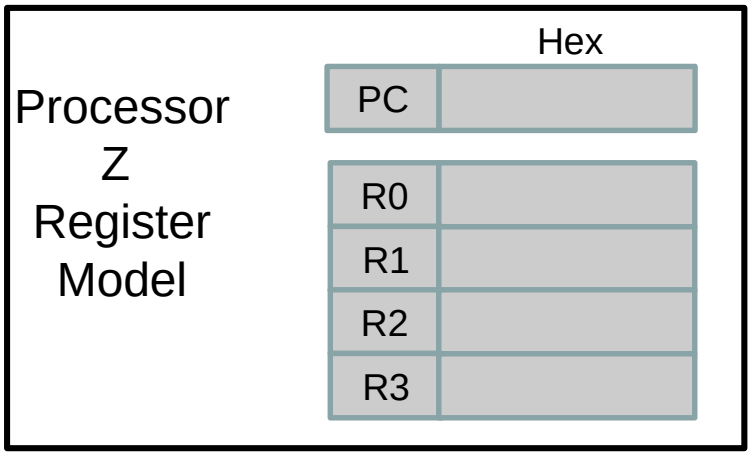
ADDRESS						DATA	
Hex						Hex	
0	0	0	0			A	D
0	0	0	1			2	1
0	0	0	2			F	6
0	0	0	3			4	1
0	0	0	4			6	0
0	0	0	5			0	9
0	0	0	6			F	F

9) Fill in the Processor Z Register model following the execution of this program snippit – 10pts

```
        org     $100A (next instruction starts at location 0x100A)

        ldi     R1,11
        ldi     R2,0x06
loop    dec     R1
        dec     R2
        bnz     R2,loop
        ldi     R3,0x03
```

Assuming 1 clock / instruction,
how many clock cycles are used?



10 – Write Processor Z assembly code to subtract lownum from highnum where lownum is in memory location 0x0200 and highnum is in memory location 0x0C02. The result should be stored in memory location 0x0C04 – 10pts

(you can assume highnum > lownum and lownum > 0)