ELE 455

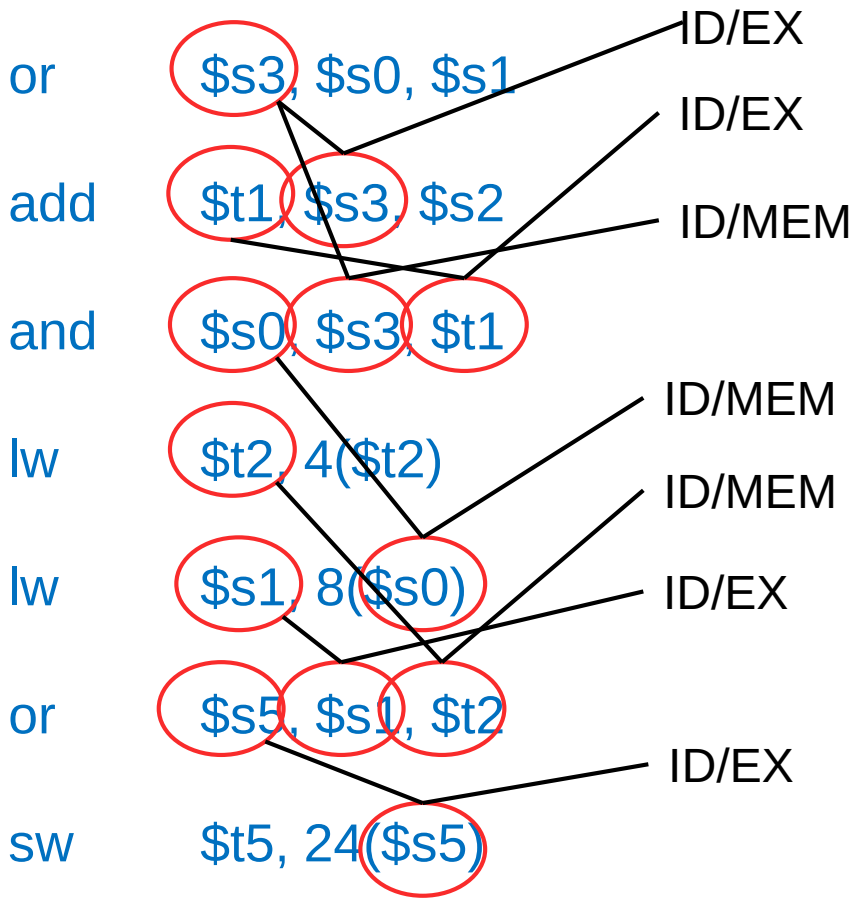
Spring 2016

Homework 5

Due 3/8

Beginning of class

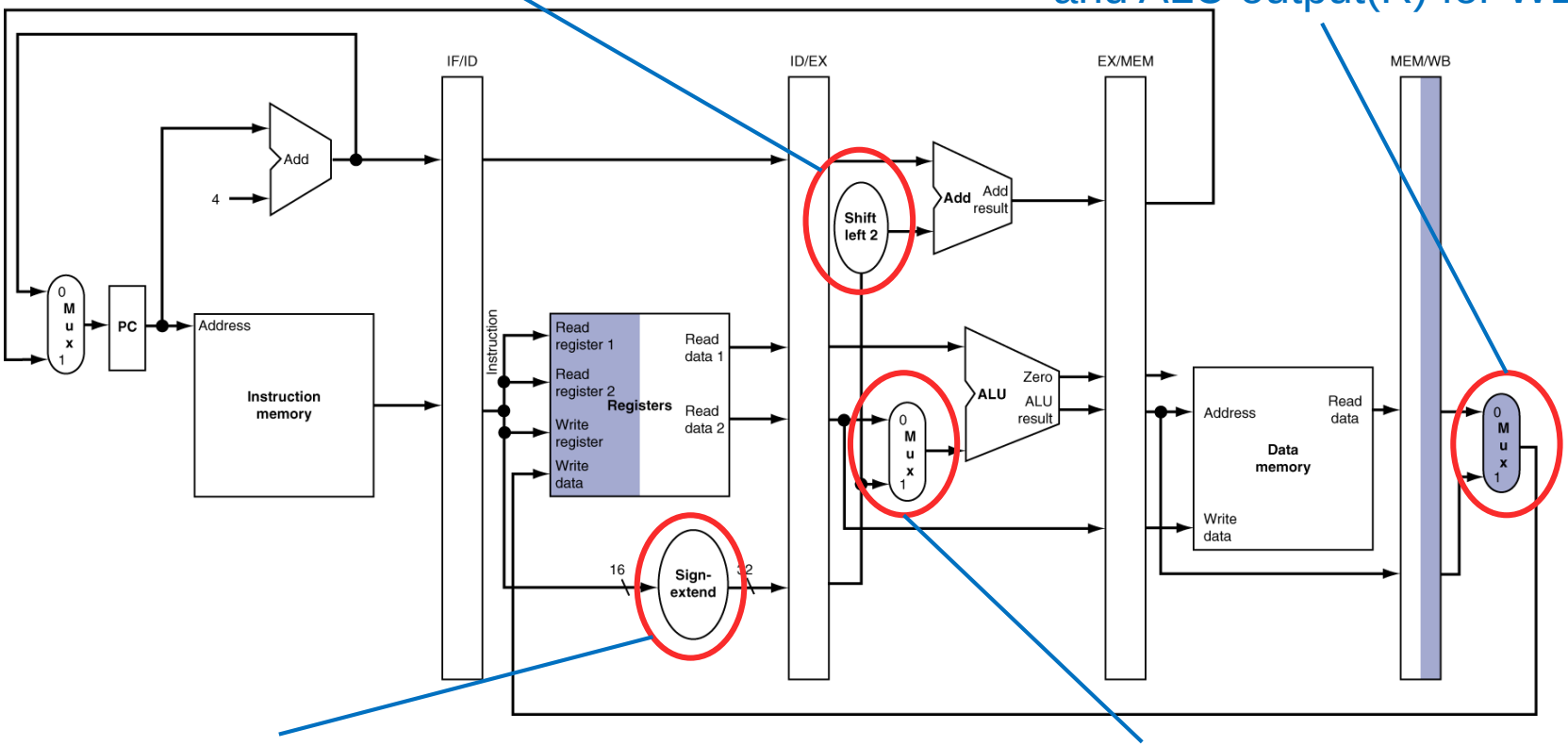
1) Assuming our standard pipeline – with no forwarding HW – indicate all the hazards along with their type (ID/EX, ID/MEM, …) in the code sequence below - 10pts



1) In the pipeline below – indicate the function of the circled blocks and explain why this configuration fails to work properly - 10pts

Multiply by 4 for 4 bytes / instruction

Choose between memory output (LS) and ALU output(R) for WB



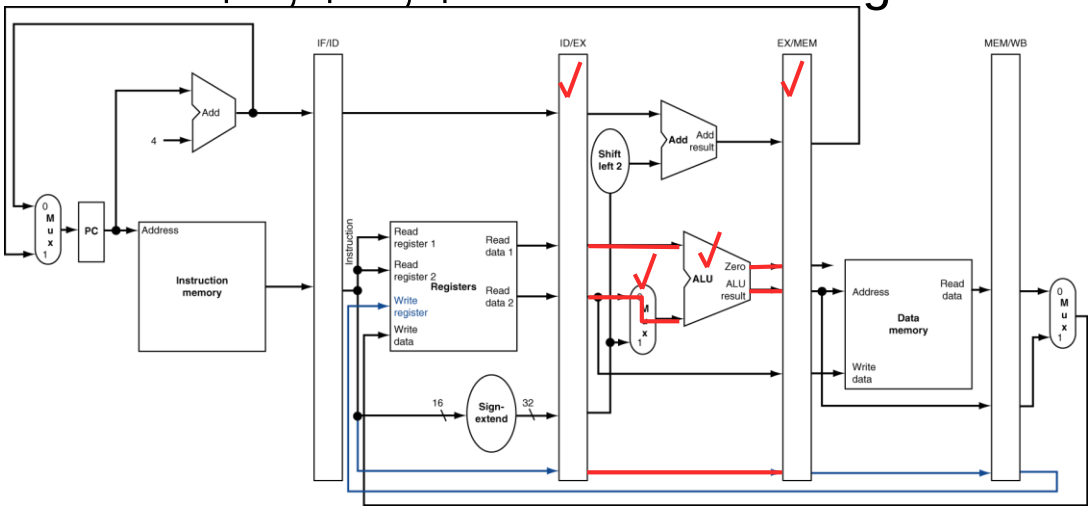
Sign extend the immediate field to 32 bits

Choose between Rt (for R type instructions) and the immediate field (for I type instructions)

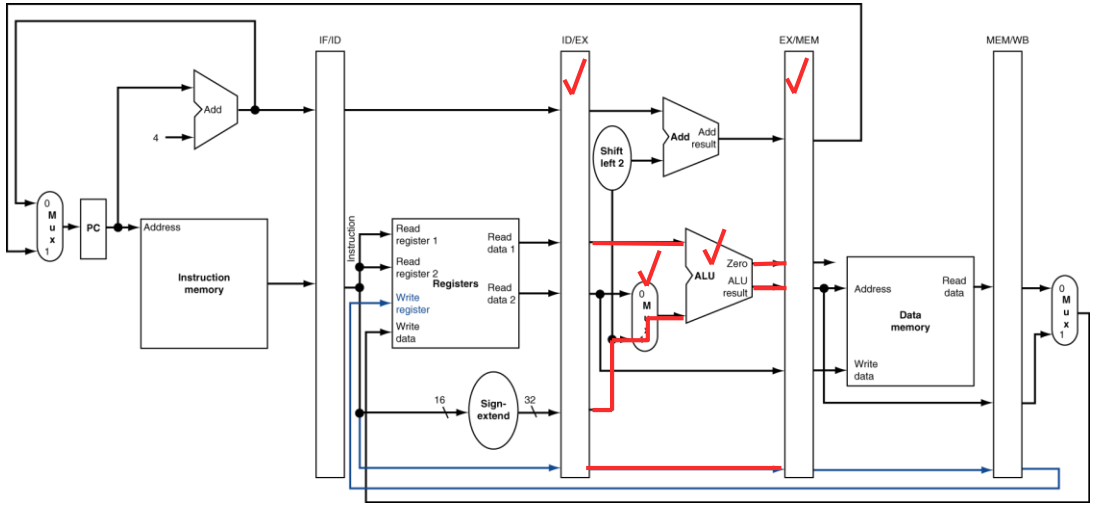
This architecture fails because the WB register address is not correctly tied to the instruction in the WB stage

2) In the pipeline below – which blocks and which paths are active for the instruction - 10pts

add $t2, $s0, $s1 in the EX stage



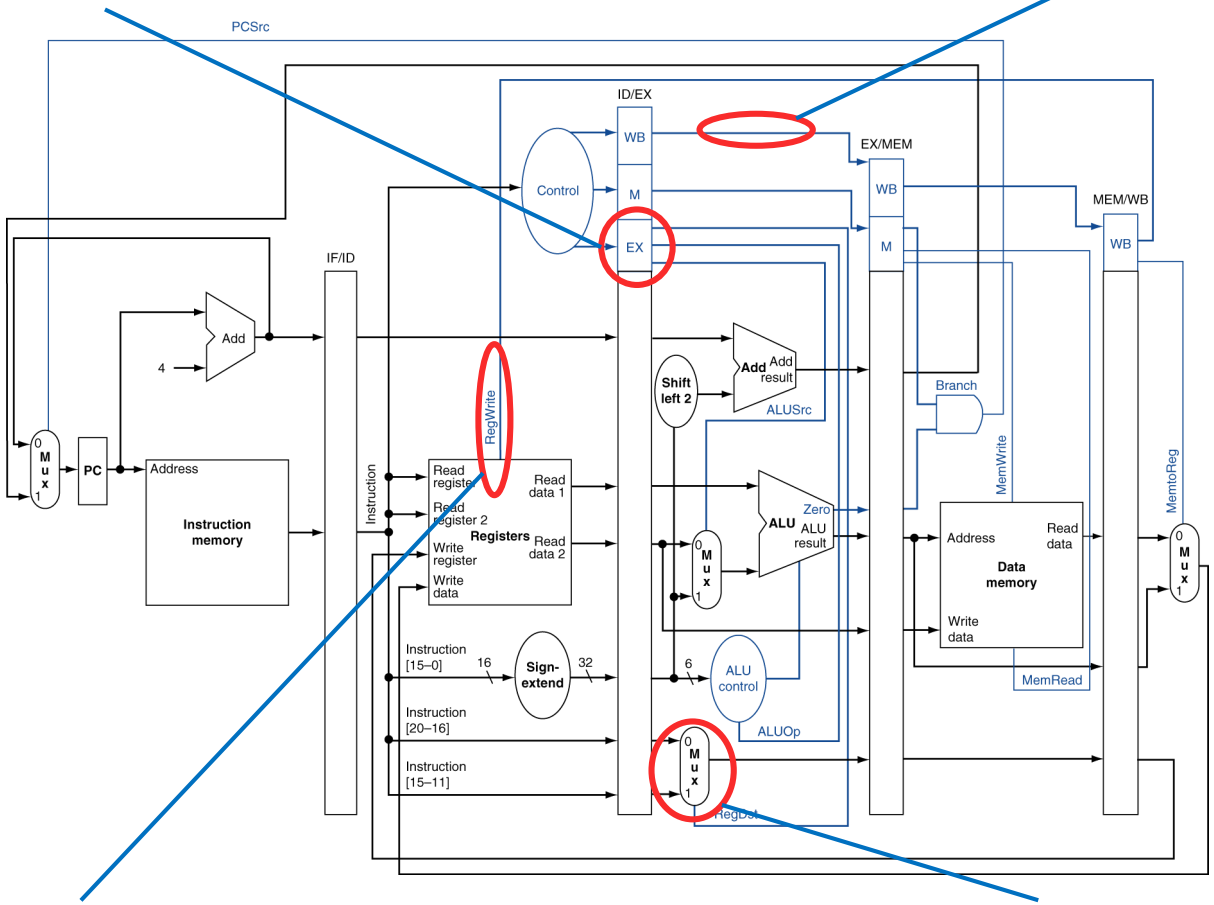
addi $t2, $s0, 29 in the EX stage



3) In the pipeline below – explain the need for the circled blocks or signals - 10pts

ID/EX register to hold the EX stage control values

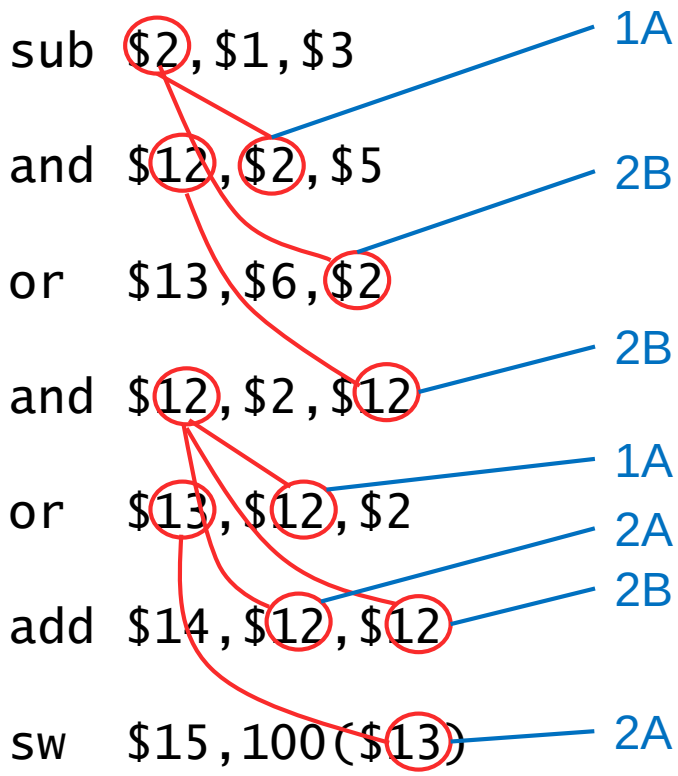
REGwrite and MemtoReg signals associated with the instruction in the EX stage



REGwrite signal associated with the instruction in the WB stage

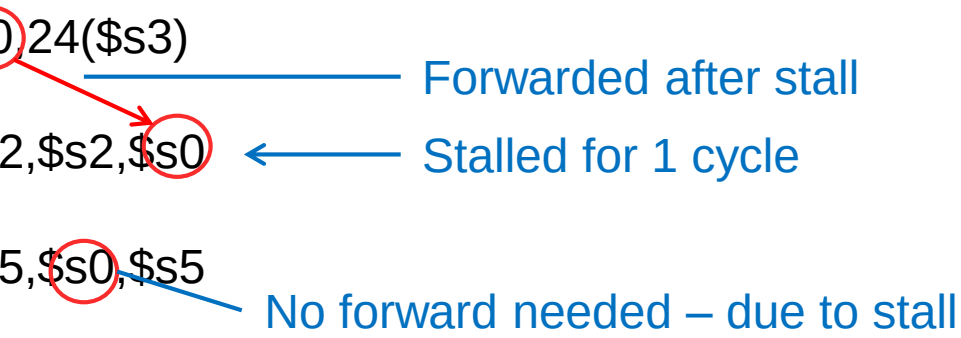
Mux to choose between the Rt and Rd field for the WB register address

4) Identify the hazards and type of each hazard below (type: 1a, 1b, 2a, 2b) - 10pts



5) Assuming our pipelined solution with forwarding, indicate which values will be forwarded in this code, also indicate which if any instructions will be stalled - 10pts

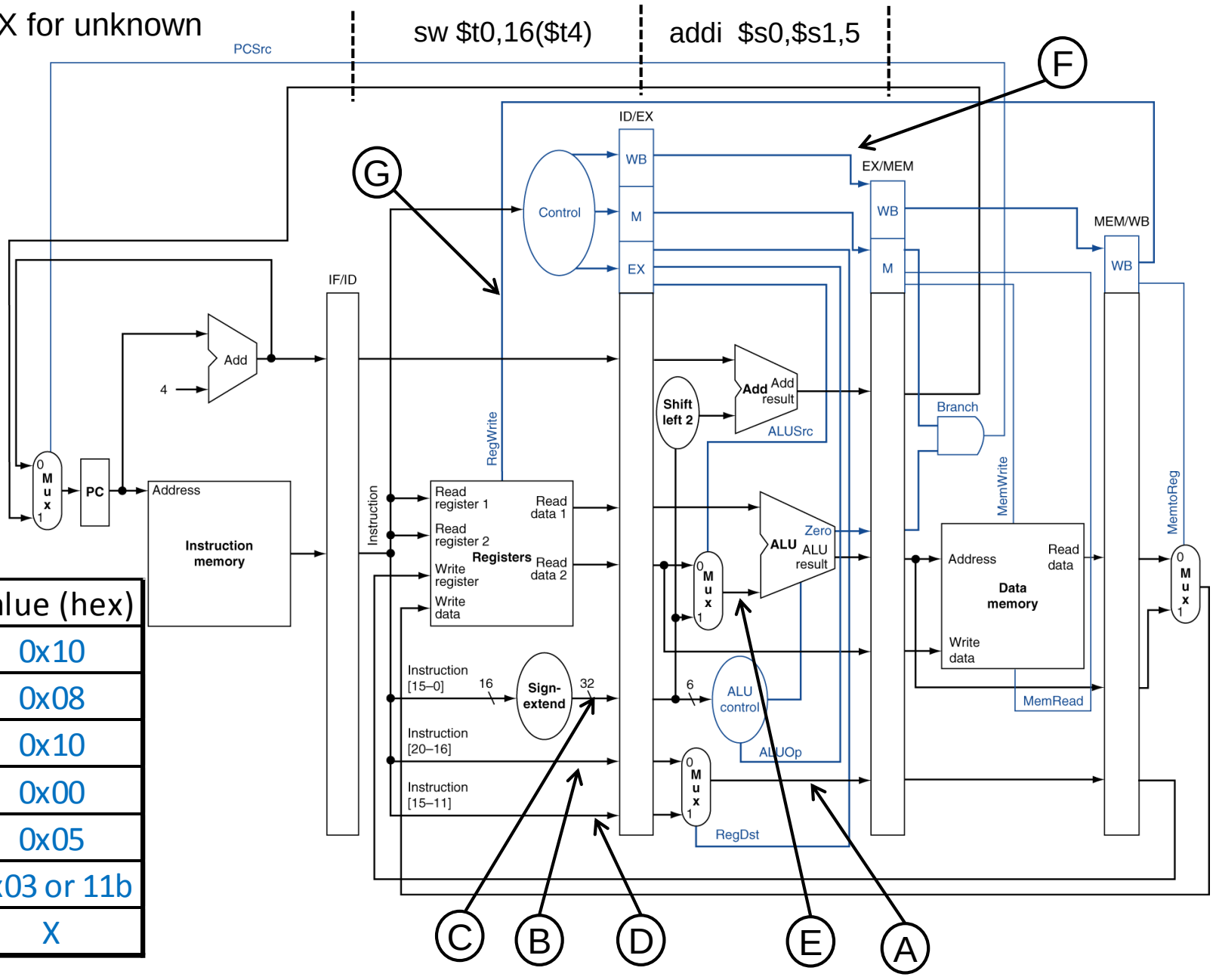
```
and  $s5, $t8, $t3

lw  $s0,24($s3)

add $t2,$s2,$s0

and $t5,$s0,$s5

or  $t3,$s5,$s0

add $t4,$t2,$t2
```



6. At the end of the clock cycle indicate the value of each data bus - 14pts

use X for unknown

Before 1st inst entered pipeline
$s0=0x2323
$s1=0x2323
$t0=0x1234
$t4=0x4321

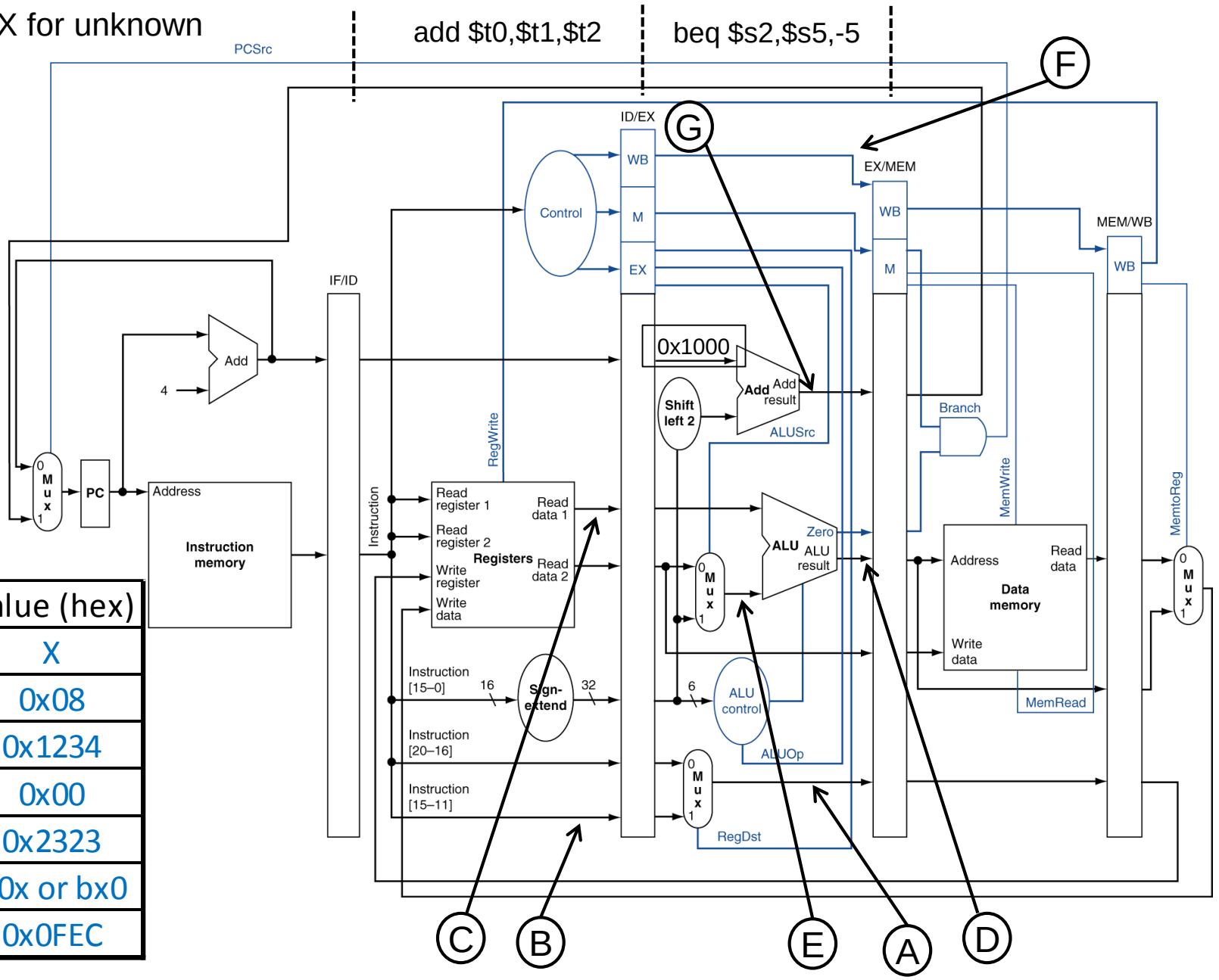


Bus	Value (hex)
A	0x10
B	0x08
C	0x10
D	0x00
E	0x05
F	0x03 or 11b
G	X

7. At the end of the clock cycle indicate the value of each data bus - 14pts

use X for unknown

Before 1st inst entered pipeline
$s2=0x2323
$s5=0x2323
$t1=0x1234
$t2=0x4321
$t0=0x1111

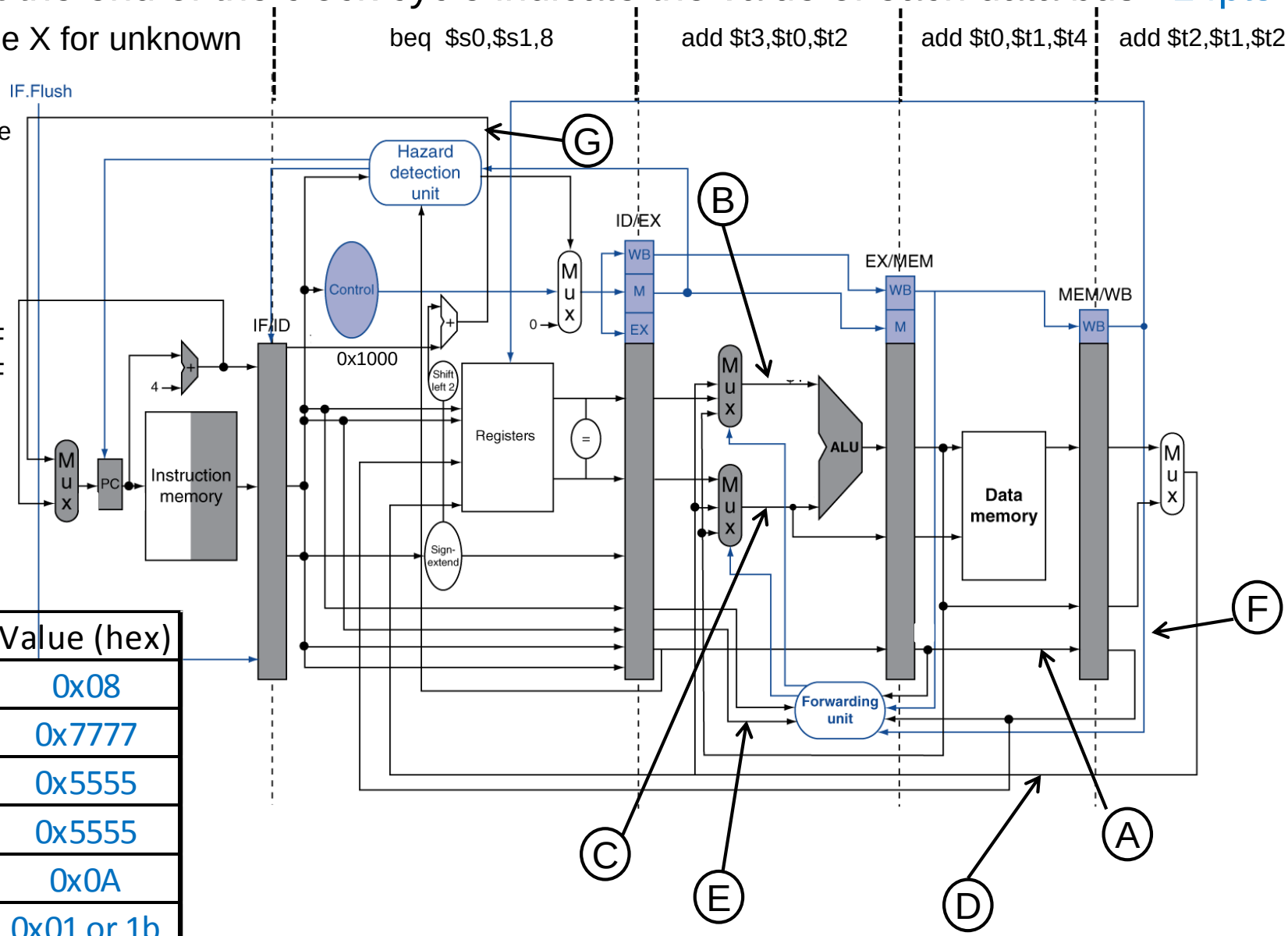


Bus	Value (hex)
A	X
B	0x08
C	0x1234
D	0x00
E	0x2323
F	b0x or bx0
G	0x0FEC

8. At the end of the clock cycle indicate the value of each data bus - 14pts

use X for unknown

Before 1st inst entered pipeline
$t0=0x1111
$t1=0x2222
$t2=0x3333
$t3=0x4444
$t4=0x5555
$s0=0xAAAF
$s1=0xAAAF



Bus	Value (hex)
A	0x08
B	0x7777
C	0x5555
D	0x5555
E	0x0A
F	0x01 or 1b
G	0x1020

9) Answer the following assuming a 2 bit dynamic branch prediction system with a 512 word deep branch prediction table with 0 indicating do not take the branch and 1 indicating take the branch (32bit word) - 10pts

With a 16Mbyte program space – what is the maximum number of possible address conflicts for any given table location

Assuming MIPS = 16MByte → 4Mwords

4MW/0.5KW = 8KW

With a uniform 6.25% branch instruction density, what is the likely number of address conflicts

.0625*8K = 512

Fill in the table (assume 11, 10, 01, 00 for the states starting upper left and rotating clockwise from lecture 4, page 42_

current state		current branch decision	next state	
0	0	taken	0	1
1	0	taken	1	1
1	1	not taken	1	0
1	0	not taken	0	1

10) Provide short answers to the following - 10pts

What is the difference between an exception and an interrupt?

Exceptions are internally generated within the CPU
Interrupts are generated outside the CPU and possibly outside the chip

Give an example of each:

A/D complete – Interrupt
Undefined instruction – exception

What is a “cause register”?

A register used to indicate the cause of an exception or interrupt
typically 1 bit for each type

What is a “reservation station”?

A holding area for instructions where they wait until all needed operands are available and valid

What is a “commit unit”?

A holding are for results where they wait pending confirmation that all predictions were correct and the values are valid