

ELE 455  
Spring 2016

Homework 5

Due 3/8  
Beginning of class

1) Assuming our standard pipeline – with no forwarding HW – indicate all the hazards along with their type (ID/EX, ID/MEM, ...) in the code sequence below - 10pts

or      \$s3, \$s0, \$s1

add     \$t1, \$s3, \$s2

and     \$s0, \$s3, \$t1

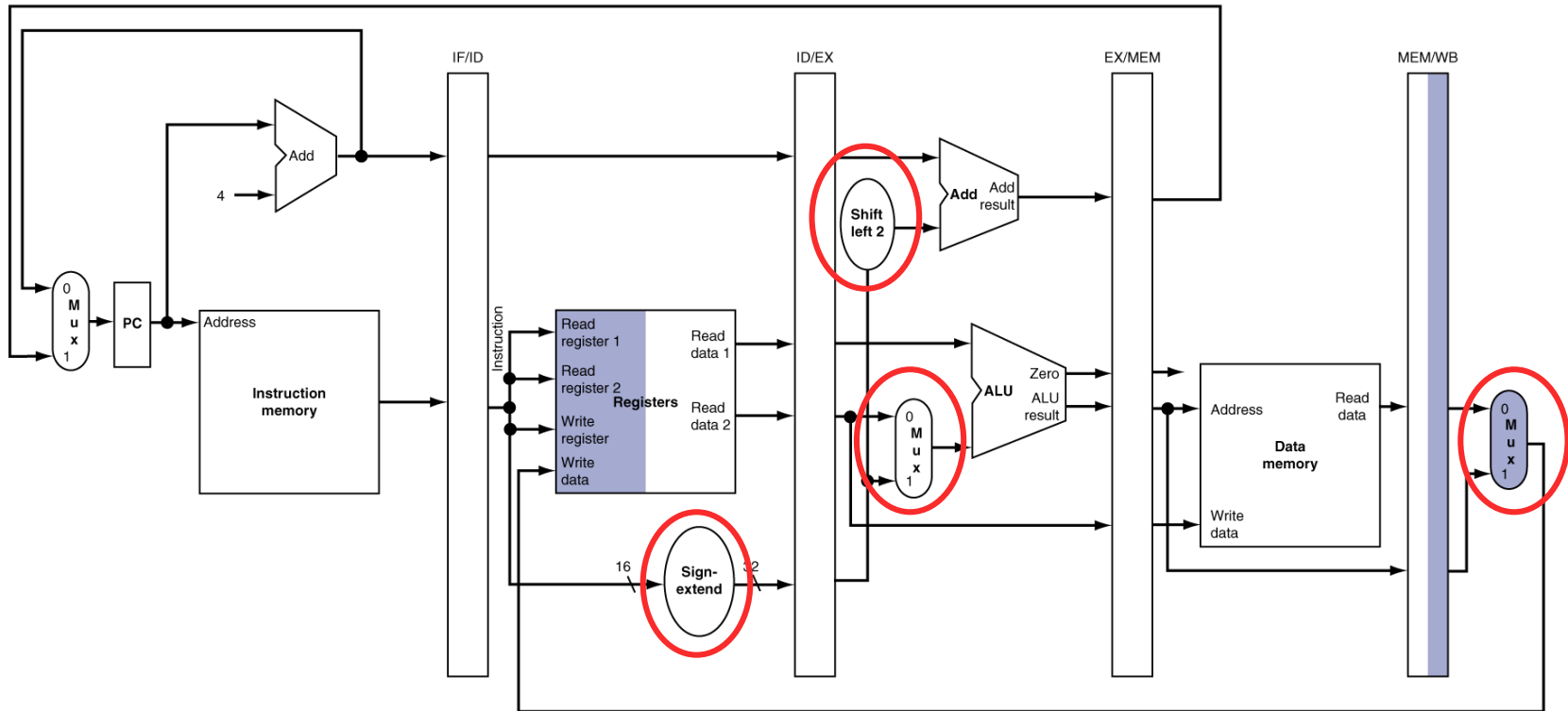
lw      \$t2, 4(\$t2)

lw      \$s1, 8(\$s0)

or      \$s5, \$s1, \$t2

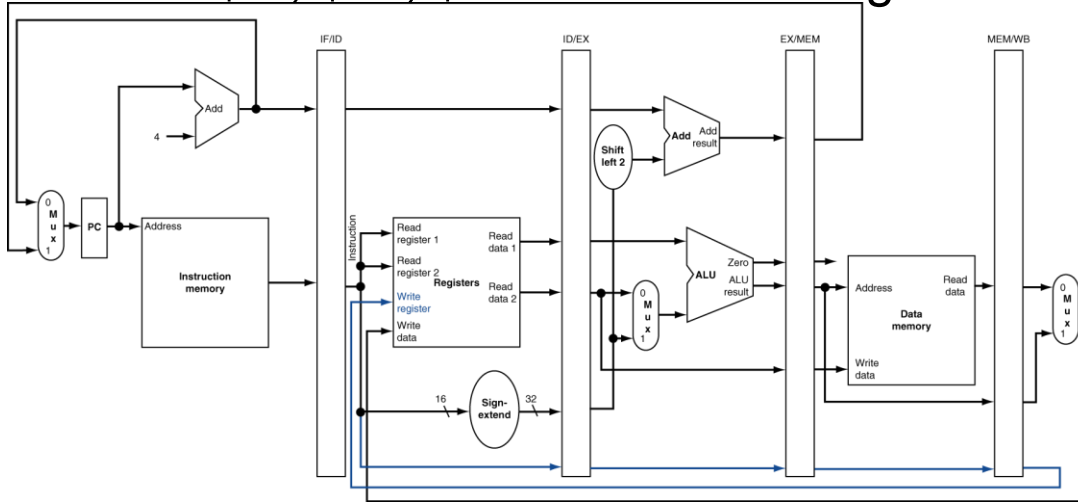
sw      \$t5, 24(\$s5)

2) In the pipeline below – indicate the function of the circled blocks and explain why this configuration fails to work properly - 10pts

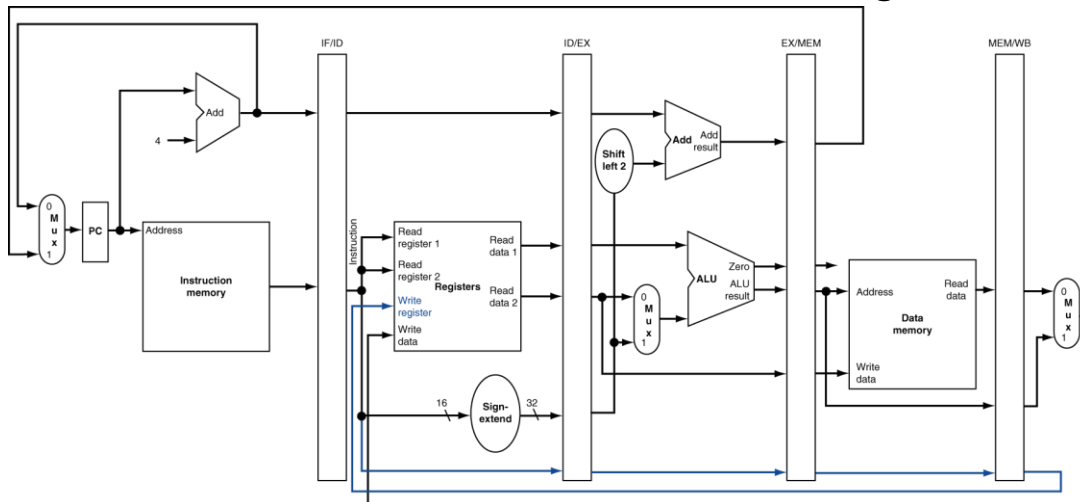


3) In the pipeline below – which blocks and which paths are active for the instruction - 10pts

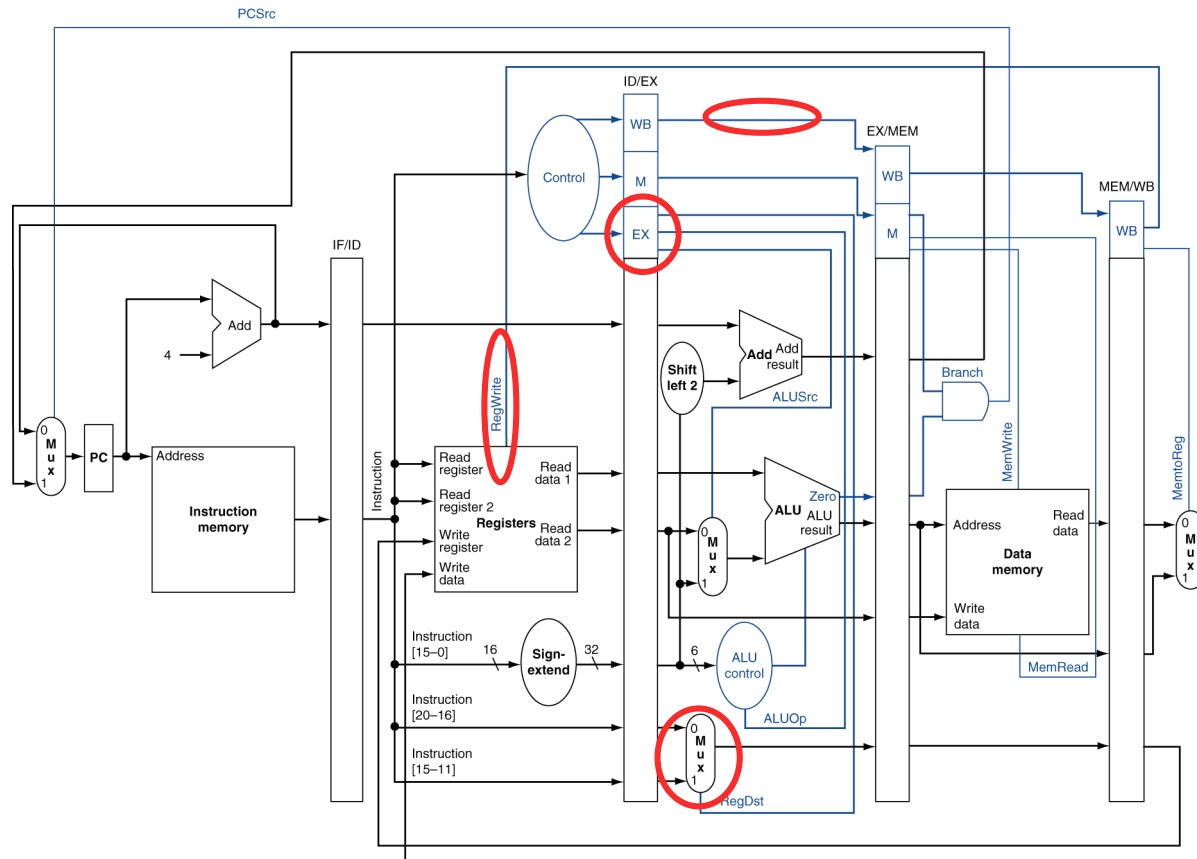
add \$t2, \$s0, \$s1 in the EX stage



addi \$t2, \$s0, 29 in the EX stage



4) In the pipeline below – explain the need for the circled blocks or signals - 10pts



5) Identify the hazards and type of each hazard below (type: 1a, 1b, 2a, 2b) - 10pts

sub \$2, \$1, \$3

and \$12, \$2, \$5

or \$13, \$6, \$2

and \$12, \$2, \$12

or \$13, \$12, \$2

add \$14, \$12, \$12

sw \$15, 100(\$13)

6) Assuming our pipelined solution with forwarding, indicate which values will be forwarded in this code, also indicate which if any instructions will be stalled - 10pts

and \$s5, \$t8, \$t3

lw \$s0,24(\$s3)

add \$t2,\$s2,\$s0

and \$t5,\$s0,\$s5

or \$t3,\$s5,\$s0

add \$t4,\$t2,\$t2

# 7. At the end of the clock cycle indicate the value of each data bus - 10pts

use X for unknown

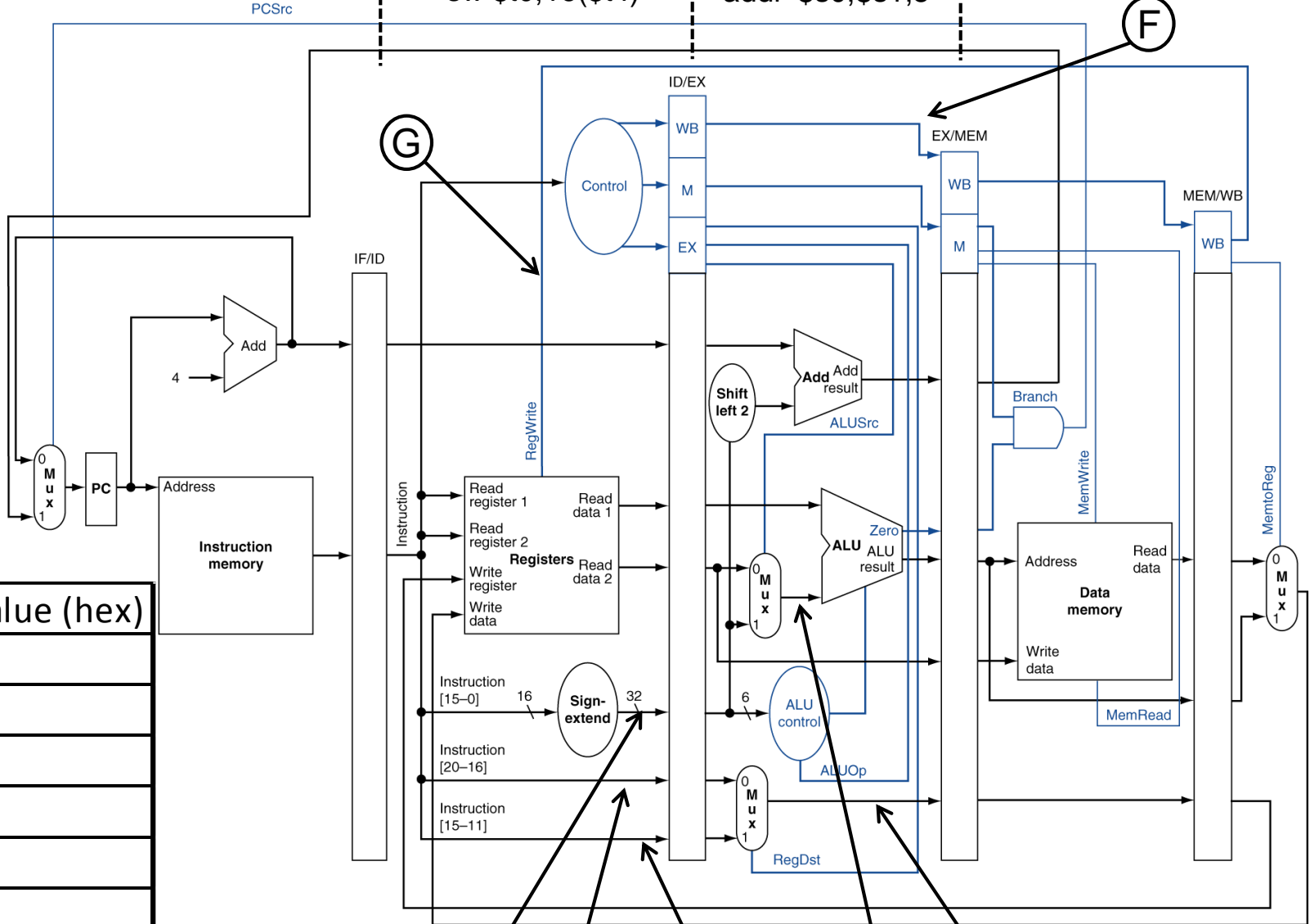
sw \$t0,16(\$t4)

addi \$s0,\$s1,5

F

G

Before 1<sup>st</sup> inst entered pipeline  
 \$s0=0x2323  
 \$s1=0x2323  
 \$t0=0x1234  
 \$t4=0x4321



Bus	Value (hex)
A	
B	
C	
D	
E	
F	
G	

C

B

D

E

A



# 8. At the end of the clock cycle indicate the value of each data bus - 10pts

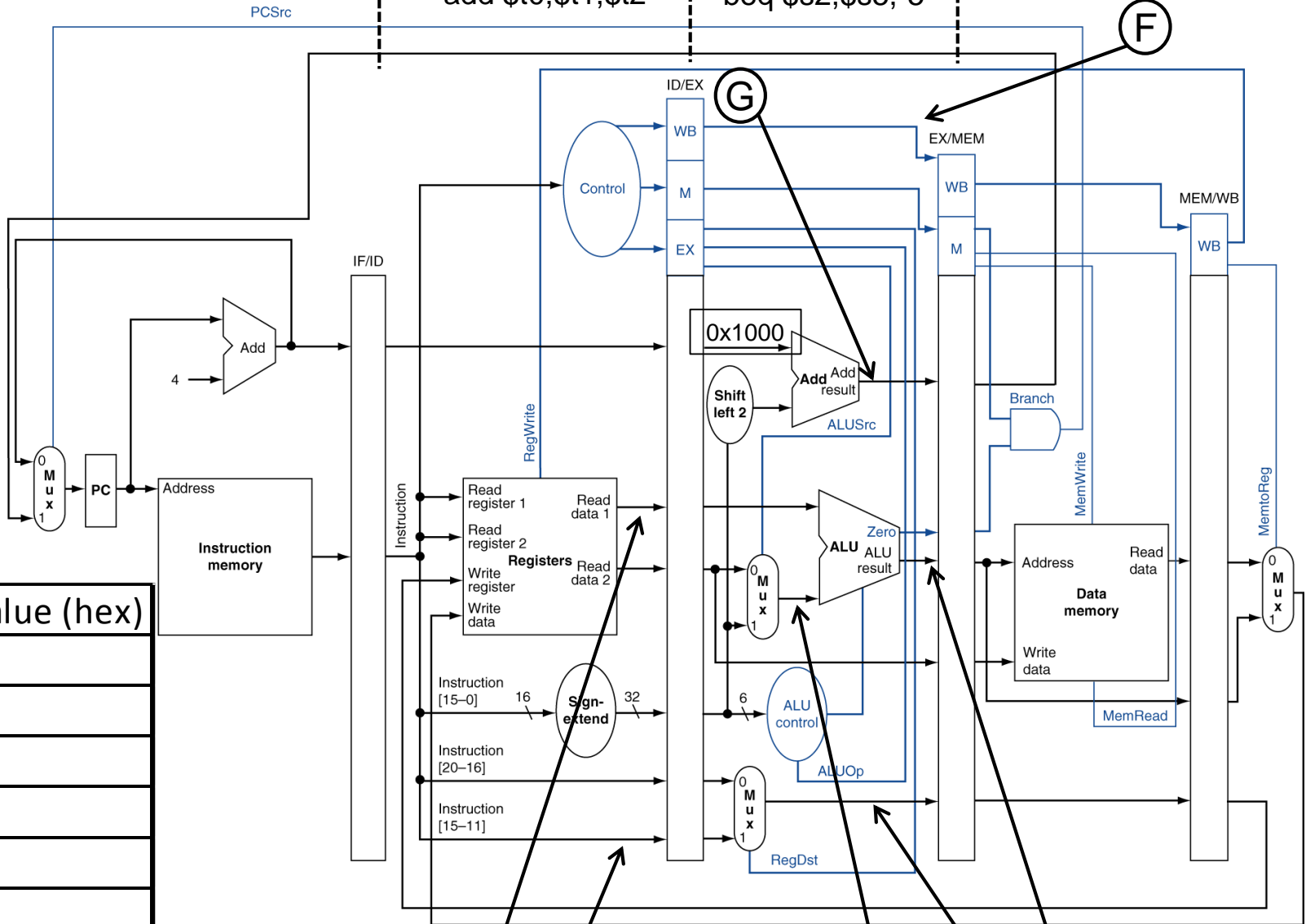
use X for unknown

add \$t0,\$t1,\$t2

beq \$s2,\$s5,-5

F

Before 1<sup>st</sup> inst entered pipeline  
 \$s2=0x2323  
 \$s5=0x2323  
 \$t1=0x1234  
 \$t2=0x4321  
 \$t0=0x1111



Bus	Value (hex)
A	
B	
C	
D	
E	
F	
G	

C B E A D

# 9. At the end of the clock cycle indicate the value of each data bus - 10pts

use X for unknown

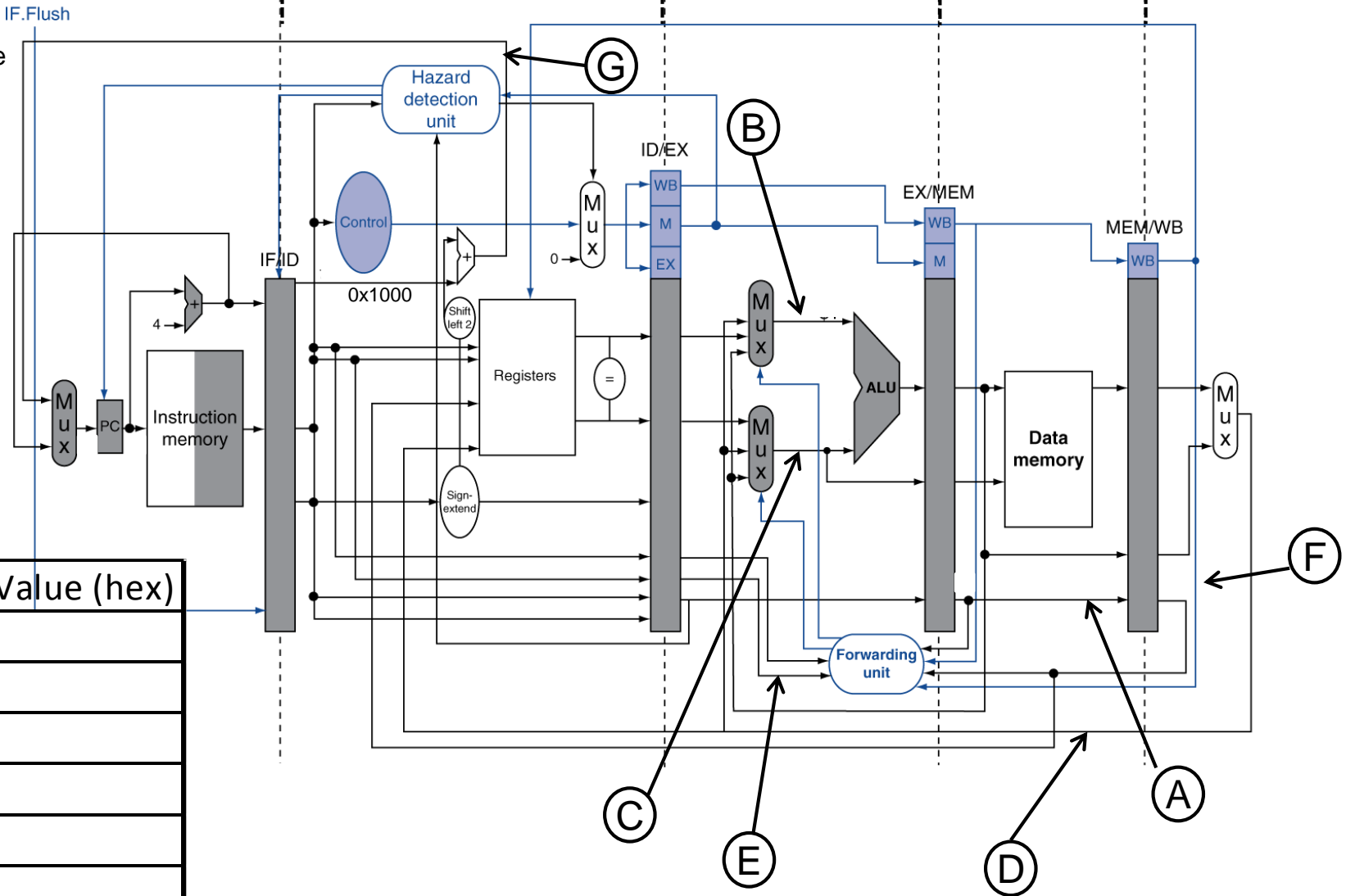
beq \$s0,\$s1,8

add \$t3,\$t0,\$t2

add \$t0,\$t1,\$t4

add \$t2,\$t1,\$t2

Before 1st inst entered pipeline  
 \$t0=0x1111  
 \$t1=0x2222  
 \$t2=0x3333  
 \$t3=0x4444  
 \$t4=0x5555  
 \$s0=0xAAAF  
 \$s1=0xAAAF



Bus	Value (hex)
A	
B	
C	
D	
E	
F	
G	

10) Answer the following assuming a 2 bit dynamic branch prediction system with a 512 word deep branch prediction table with 0 indicating do not take the branch and 1 indicating take the branch (32bit word) - 10pts

With a 16Mbyte program space – what is the maximum number of possible address conflicts for any given table location

With a uniform 6.25% branch instruction density, what is the likely number of address conflicts

Fill in the table (assume 11, 10, 01, 00 for the states starting upper left and rotating clockwise from lecture 4, page 42\_

current state		current branch decision	next state	
0	0	taken		
1	0	taken		
1	1	not taken		
1	0	not taken		