ELE 455/555

# Spring 2016

Homework 6

Due 3/29/2016

Beginning of class

1) Consider the three Micron SDRAM data sheets on the website – Indicate the number of clock cycles required to read 8, 32 bit words from each part in the x16 version - 10 pts
assume a burst read – (no latency time included)

| Part | # clocks |
|---|---|
| DDR | |
| DDR2 | |
| DDR3 | |

2) Consider the 3 Micron SDRAM data sheets on the website – Indicate
a) the maximum clock frequency for each
b) the amount of time required to read 8, 32 bit words from each part in the x16 version running at max clock frequency - 20 pts
assume a burst read – (no latency time included)

3) Given an empty 8 block direct mapped cache, indicate: - 15 pts

a) Which memory accesses are “hits” and “misses”

b) Fill in the final cache table below

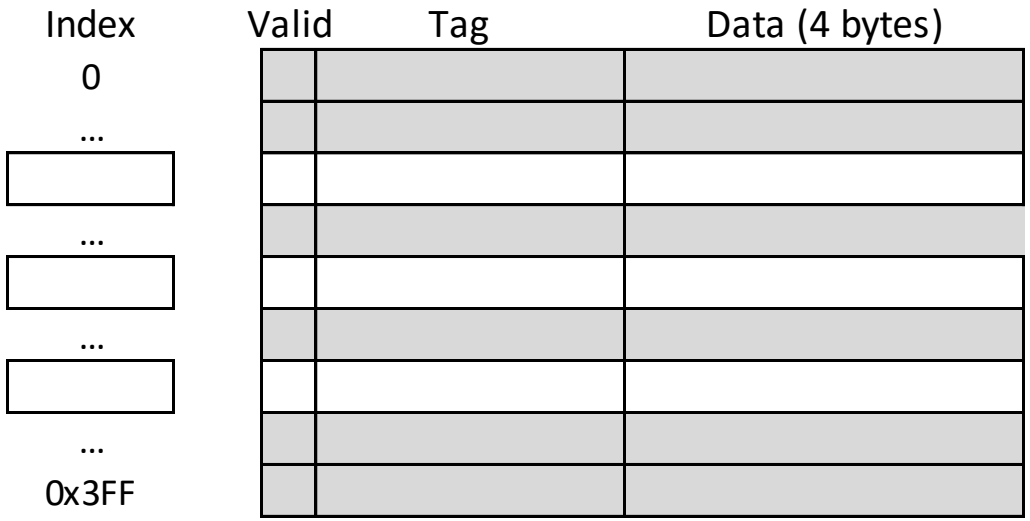
| Memory Reference (decimal) | Hit or Miss |
|---|---|
| 22 | |
| 26 | |
| 3 | |
| 22 | |
| 18 | |
| 3 | |
| 26 | |
| 18 | |

| Index (binary) | V | Tag (binary) | Data mem(xxxxxb) |
|---|---|---|---|
| | | | |
| | | | |
| | | | |
| | | | |
| | | | |
| | | | |
| | | | |
| | | | |

4) Given an 1K block direct mapped cache and a 20 bit address space, fill in the table below, given the following memory references (assume 32 bit words) - 15 pts

| Memory Location (hex) | Data value (hex) |
|---|---|
| 3B2B4 | 0x12212345 |
| 699FC | 0x0110ABCD |
| 83158 | 0xFFEE9876 |

use HEX for all values



5) Calculate the total number of bits in a 32KB direct mapped cache assume 16 word blocks, 32 bit words, and a 32bit address space – you must show work to get credit - 20 pts

6) Using the cache from problem 5, identify which block each address maps to – you must show work to get credit - 20 pts

| Addr | Cache Block |
|---|---|
| 0x2FF324 | |
| 0xFF | |
| 0xDC3458 | |
| 0xAAA | |
| 0x12344324 | |

For prob 3 - Assume a 1 word blocks with 1 byte words

| Addr | Cache Block |
|---|---|
| 0x2FF326 | |
| 0xFE | |
| 0xDC3455 | |
| 0xAA1 | |
| 0x12344323 | |