ELE 455/555

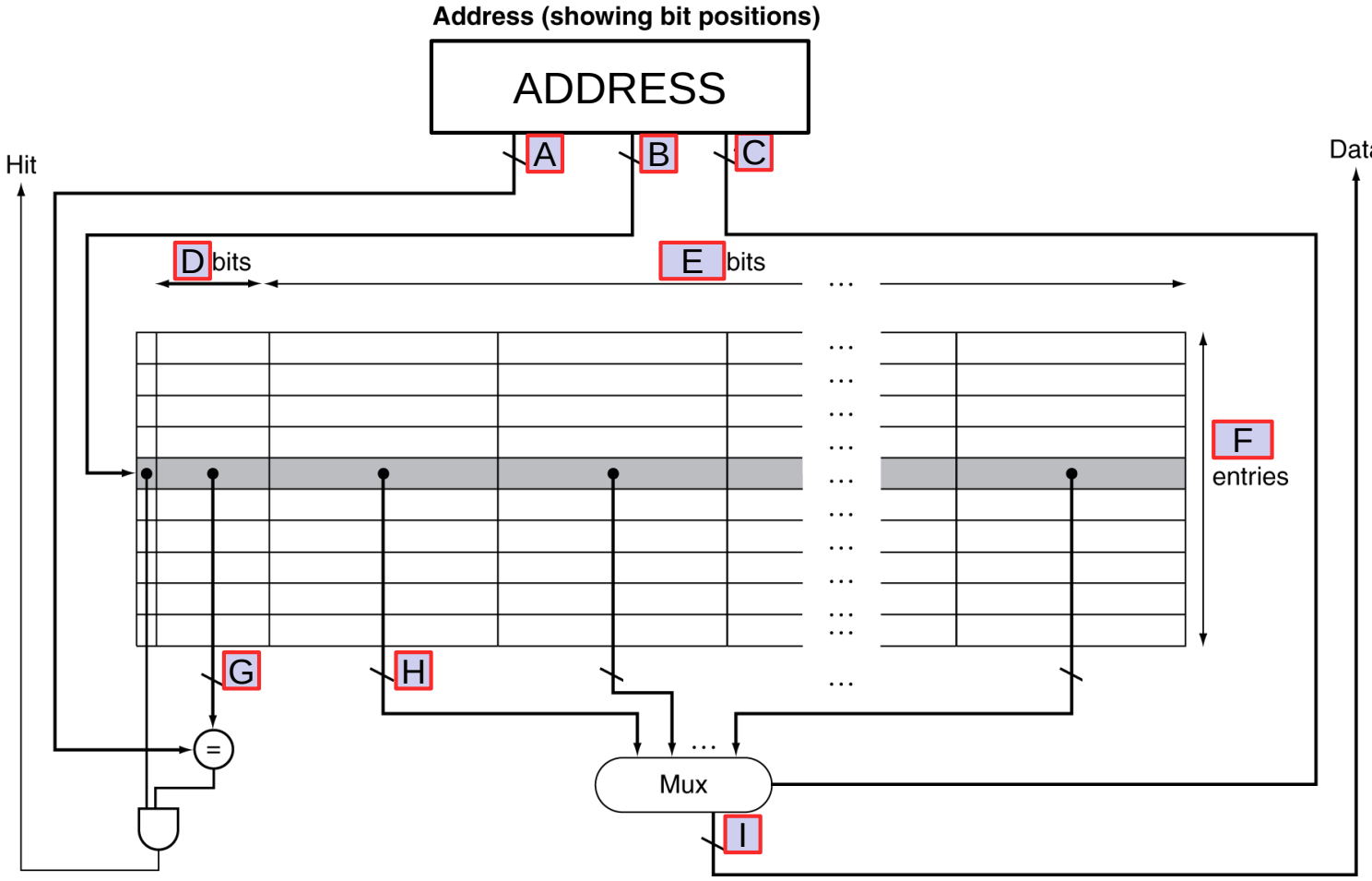
Spring 2016

Homework 7

Due 4/5/2016

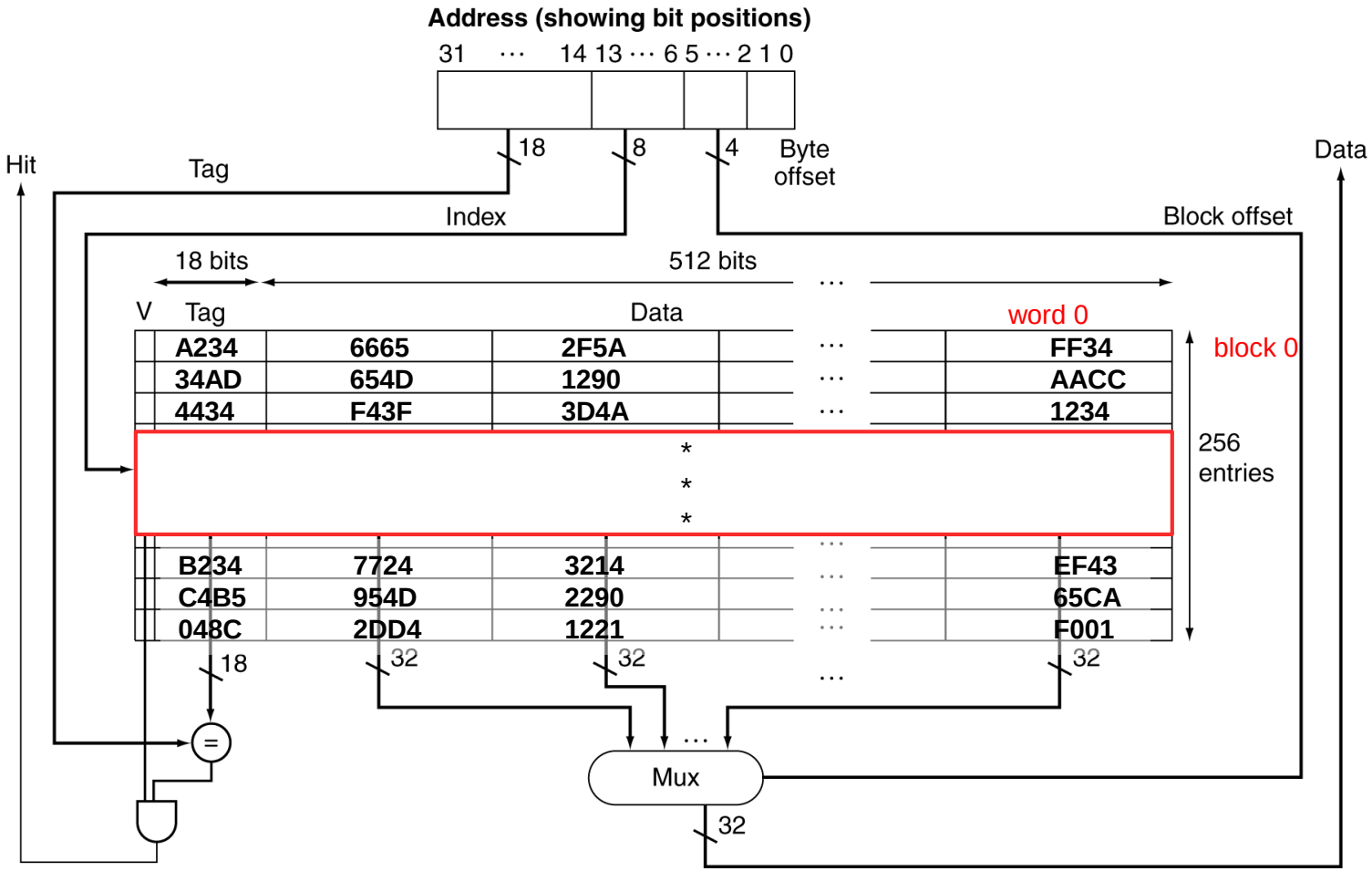
Beginning of class

1) Given a 4kB direct mapped cache with 16 bit words, 4 word blocks, and 32 bit addressing – fill in the table referencing each letter. - 15 pts



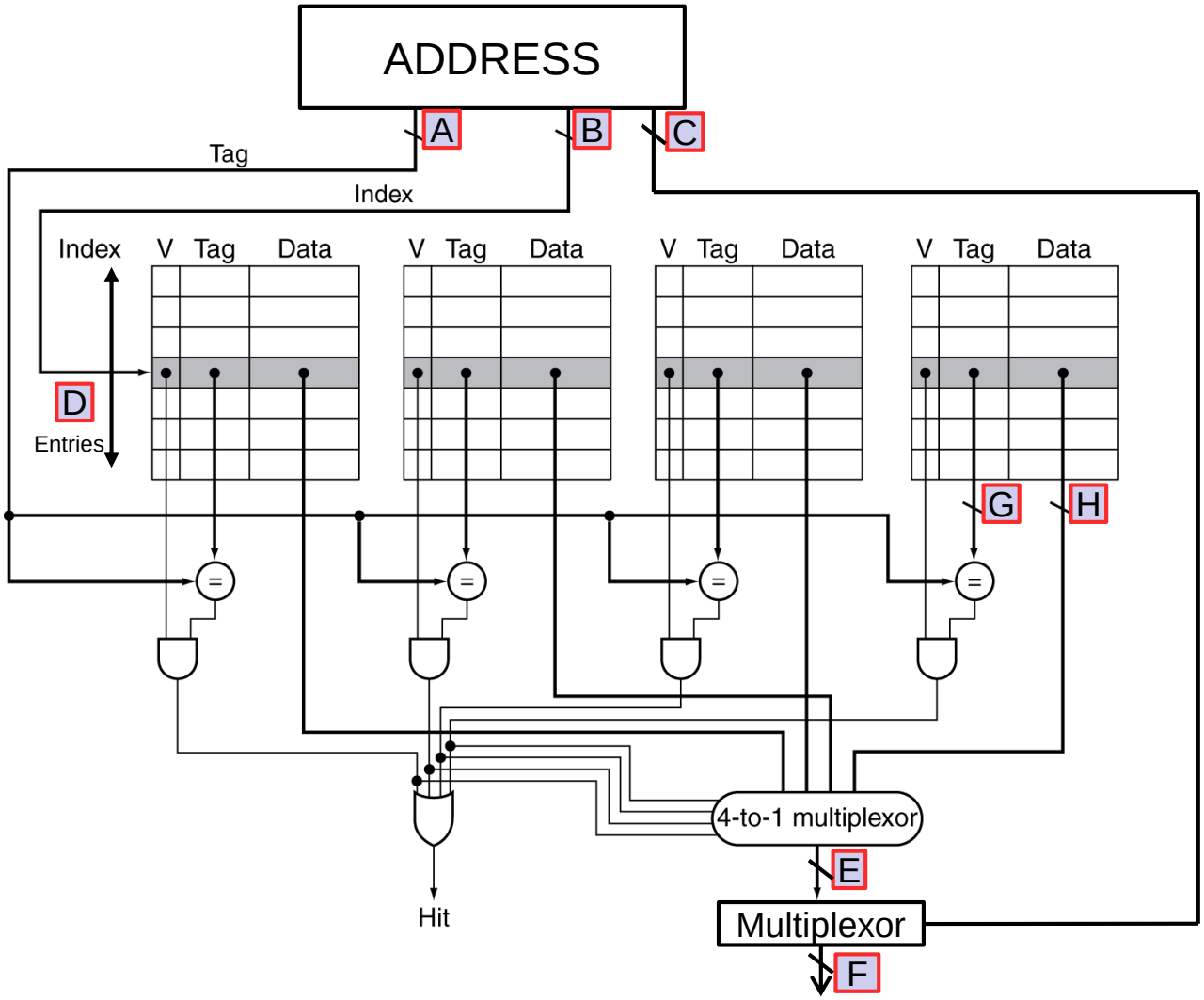
A	
B	
C	
D	
E	
F	
G	
H	
I	

2) Given the cache below – fill in the data table for each read address - 15pts
use X for unknown – all entries are HEX and all are valid



ADDR	Data	Hit (Y/N)
0D2B4040		
222F003C		
2E8D3F78		
2C8D3F78		
1233FFC		

3) Given a 32kB 4-way set associative cache with 16 bit words, 16 word blocks, and 32 bit addressing – fill in the table referencing each letter. - 15 pts



A	
B	
C	
D	
E	
F	
G	
H	

4) Given a 4 set 2-way associative cache, with 5 bit addressing and 16 bit words, starting with the cache below and using LRU for replacement indicate: Note: use block 0 for the first replacement in each set - 15 pts

a) How many misses occur with the given memory references

b) Fill in the final cache table below

Memory References (decimal)
26
6
24
4
16
4
22
6
20

4 misses

Set (binary)	V	Tag (binary)	Data
00	1	10	mem(10000,10001 b)
	1	11	mem(11000,11001 b)
01	1	00	mem(00010,00011 b)
	1	01	mem(01010,01011 b)
10	1	10	mem(10100,10101 b)
	1	11	mem(11100,11101 b)
11	1	10	mem(10110,10111 b)
	1	00	mem(00110,00111 b)

Set (binary)	V	Tag (binary)	Data
00			
01			
10			
11			

5) Calculate the total number of bits in a 64KB 8-way set associative cache assume 4 word blocks, 16 bit words, and a 64bit address space – you must show work to get credit - 15 pts

6) Calculate the effective CPI given the following: - 15 pts

$CPI_{ideal} = 1$
1.5% instruction miss rate
50 cycle instruction miss penalty
3% data miss rate
40 cycle data miss penalty
15% of instructions are loads
15% of instructions are stores
15% of instructions are add immediate

7) Which processor will have the better performance (AMAT): - 10 pts

Show the AMAT for each

A) 1Ghz clock, 4KB L1 I and D caches, 5% miss rate, 20 cycle miss penalty

B) 1.5GHz clock, 2KB L1 I and D caches, 8% miss rate, 15 cycle miss penalty