ELE 555

Spring 2016

Homework 7A

Due 4/5/2016

Beginning of class

1) Similar to problem 4 in the 455 HW:
Given an 4 set 2-way associative cache, with 5 bit addressing and 16 bit words, starting with the cache below and using LRU for replacement indicate: Note: use block 0 for the first replacement in each set - 15 pts

a) How many misses occur with the given memory references
b) Fill in the final cache table below

Memory References (decimal)
26
10
24
26
2
8
22
18
20

4 misses

Set (binary)	V	Tag (binary)	Data
00	1	10	mem(10000,10001 b)
	1	11	mem(11000,11001 b)
01	1	00	mem(00010,00011 b)
	1	01	mem(01010,01011 b)
10	1	10	mem(10100,10101 b)
	1	11	mem(11100,11101 b)
11	1	10	mem(10110,10111 b)
	1	00	mem(00110,00111 b)

Set (binary)	V	Tag (binary)	Data
00			
01			
10			
11			

2) For our technology and applications we can estimate: - 15pts

cache miss rate = 1.0% / (Cache size in KB)

cache miss cycle count = 25 * (Cache size in KB) * (Clock Freq in GHz)

a) Plot AMAT vs Cache size for 1,2,4,8,16 and 32KB cache sizes with a 1.5GHz clock frequency

b) Plot AMAT vs Clock Freq for 0.5,1 1.5,2,2.5 GHz clock frequencies with a 8KB cache

c) Comment on why these equations might make sense