ELE 455/555

Spring 2016

Homework 8

Due 4/12/2016

Beginning of Class

1) Describe each of the following. - 20 pts

TLB Hit

TLB Miss, Page Table Hit

TLB Miss, Page Table Miss

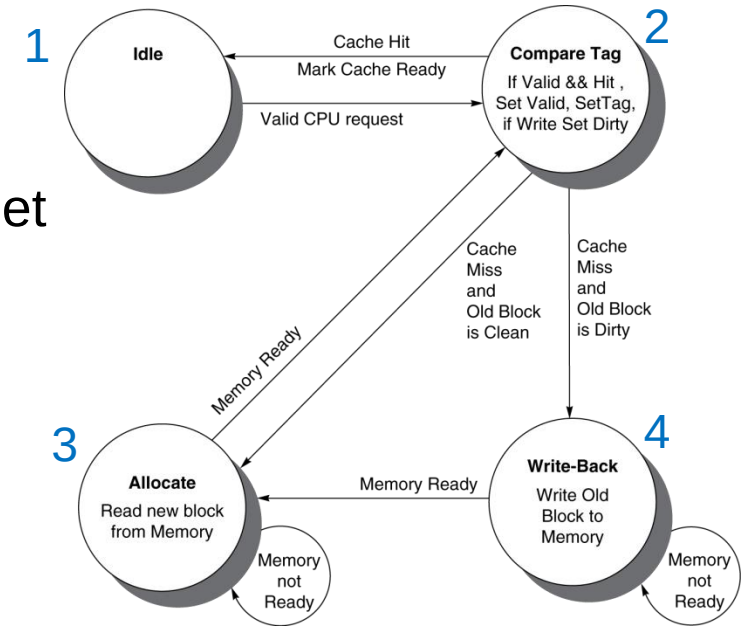
Page Fault

2) Assuming a TLB hit – which states (1,2,3,4) and in which order will the cache control transition. - 20 pts

a) On a read with a cache miss and dirty bit set

b) On a read, with a cache hit

c) On a write with a cache miss and dirty bit clear



3) Using a write-invalidate snooping protocol, indicate which memory accesses are misses or invalidates in the following sequence. Memory locations are X and Y. Assume CPUA already has Y in its cache and CPUB already has X in its cache. - 20 pts

cpuA read x
cpuA read y
cpuA write y
cpuB read y
cpuB read x
cpuA read x
cpuB write x
cpuA write x
cpuB read x

4) Provide the parity bits for the following binary values - 5 pts

Even Parity:

1001 1101
1000 0000 1101 0010
1011
1000 0101 0111 0101

Odd Parity:

1101 1101 1100 1101
1010
1001 1011
1111 0010

5) Provide the correct 12 bit value for each number – assuming 4 parity bits in the normal locations - 15 pts

Original Data		Transmitted Data											
		1	2	3	4	5	6	7	8	9	10	11	12
1101	1110												
1101	1010												
0010	1010												
1011	1101												

6) Provide the correct 8 bit value for each number – assuming 4 parity bits in the normal locations - 20 pts

Received Data			Corrected Data	
1 2 3 4	5 6 7 8	9 10 11 12		
0101	0010	1010		
1110	1010	1110		
1101	0100	1110		
0110	0100	1001		