ELE 455/555
Computer System Engineering

Section 3 – Memory

Class 1 – Memory Overview

Memory Overview

Memory Types

- Current memory systems
  - Magnetic Disk
  - Flash
  - DRAM
  - SRAM

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Memory Overview

Memory Types

- Magnetic Disk
  - Platter
    - Ferro-magnetic coating on a circular platter
      - Magneto-resistive
      - Giant Magneto-resistive
      - Tunneling Magneto-resistive
    - 2 sided
    - Magnetized by applying a magnetic field
    - Read by passing a coil over the magnetized area

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Memory Overview

Memory Types

- Magnetic Disk
  - Platter
    - Platter spins at a constant rate
      - read/write heads are semi-fixed
    - Platter is broken into annular “tracks”
    - Tracks are broken into contiguous “sectors”
    - Bits are read and written in 512K Byte sectors
    - Bit density (area) changes with respect to the distance from the center
      - Outside edge moving very quickly

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Memory Overview

Memory Types

- Magnetic Disk
  - "flying" head
    - Contains both a read and a write capability
    - Mechanically designed to:
      - Swing from outside edge to inside edge
        - Provides access to all tracks
      - Fly a few nm above the disk
        - Concept is called an "air bearing"

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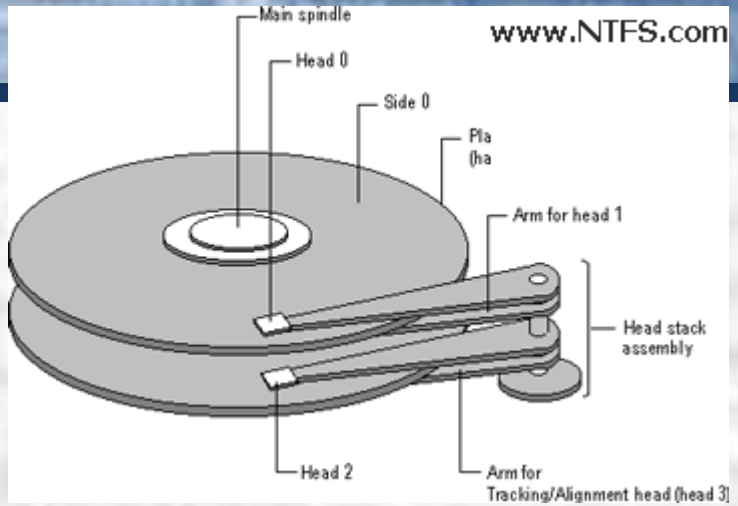
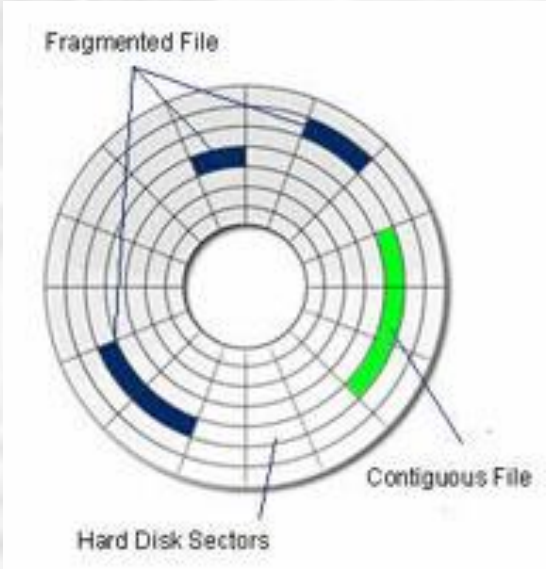
Memory Overview

Memory Types

- Magnetic Disk
  - Hard Disk Drive
    - 2.6” to 3.7” platters
      - Mobile devices down to 0.75”
    - 1-5 platters / drive
    - 1000s of tracks / platter





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Memory Overview

Memory Types

- Magnetic Disk
  - Hard Disk Drive
  - Specifications
    - 2TByte data storage
    - 5400 rpm platter rotation
    - 12ms seek time – time to randomly access a sector
    - 8MByte buffer
    - $100
      - 50nCents / Kbyte

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Memory Overview

Memory Types

- Flash
  - Future addition
  - Not common in “computer” systems

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Memory Overview

Memory Types

- SDRAM
  - Capacitor based storage
    - Requires refresh
  - Dynamic
  - Random Access
  - Row and Column access architecture
  - Synchronous
    - Clock (and outputs)matched to processor bus
  - Burst mode
    - Allows additional bytes to be read on a single address access

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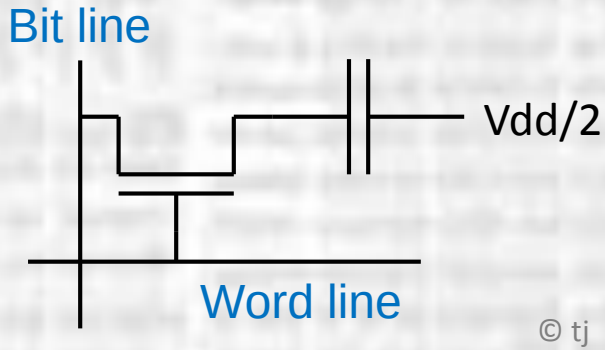
Memory Overview

Memory Types

- SDRAM – Synchronous Dynamic Random Access Memory
  - Memory cell (1 bit) is based on capacitor charge storage
  - Bit value decays over time
    - must be recharged – called a refresh cycle
  - Standard SDRAM transfers 1 word each array access
    - DDR – double data rate – transfers 2 words each array access
    - DDR2, DDR3, DDR4 – transfer 4,8,16 words each array access
  - Medium speed
  - Highest density
  - Used as main memory



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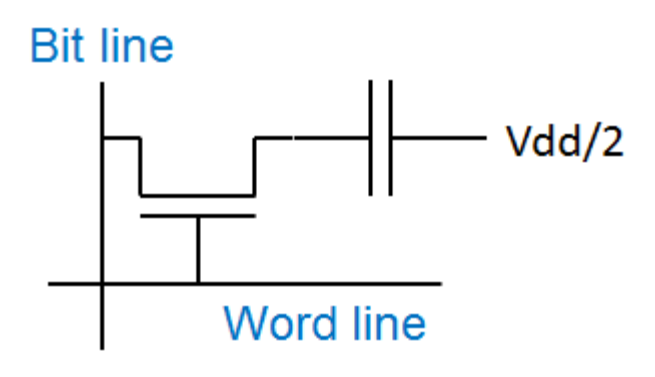
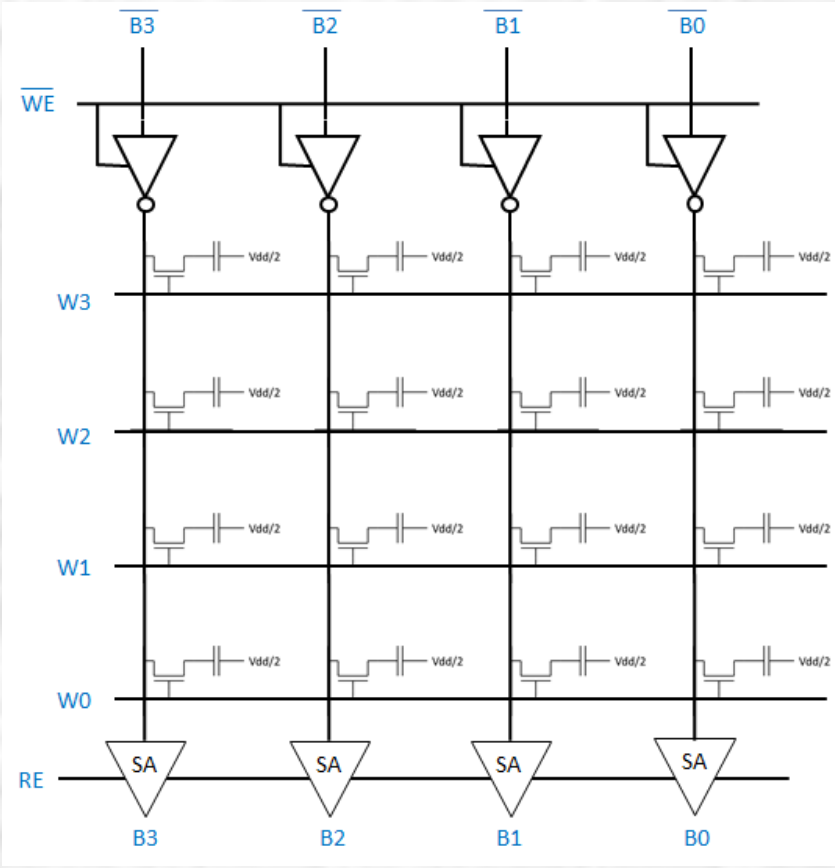
Memory Overview

Memory Types

- SDRAM – Synchronous Dynamic Random Access Memory
  - Write
    - All Word lines low
    - Read Enable (RE) disabled (low)
    - Place B0, B1, B2, B3 on inputs
    - Pull write enable bar (WE) low
    - Strobe the desired word line high
    - Bit lines write to the bit cell capacitors





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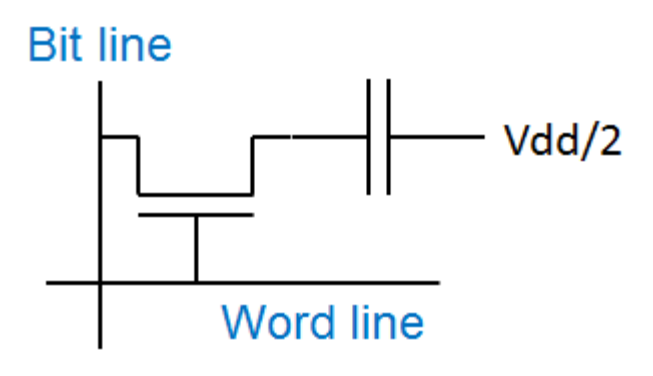
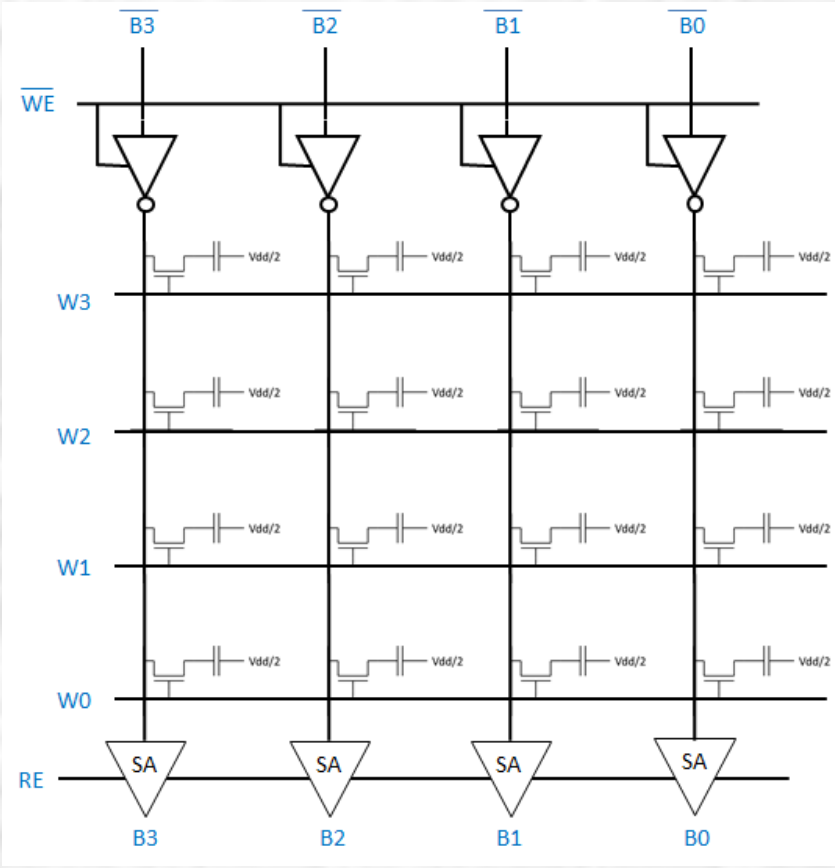
Memory Overview

Memory Types

- SDRAM – Synchronous Dynamic Random Access Memory
  - Read
    - All Word lines low
    - Write enable bar (WE) high
      - inverters tristated
    - Read Enable (RE) high
    - Strobe the desired word line high
    - Sense amplifiers read the value of the capacitors





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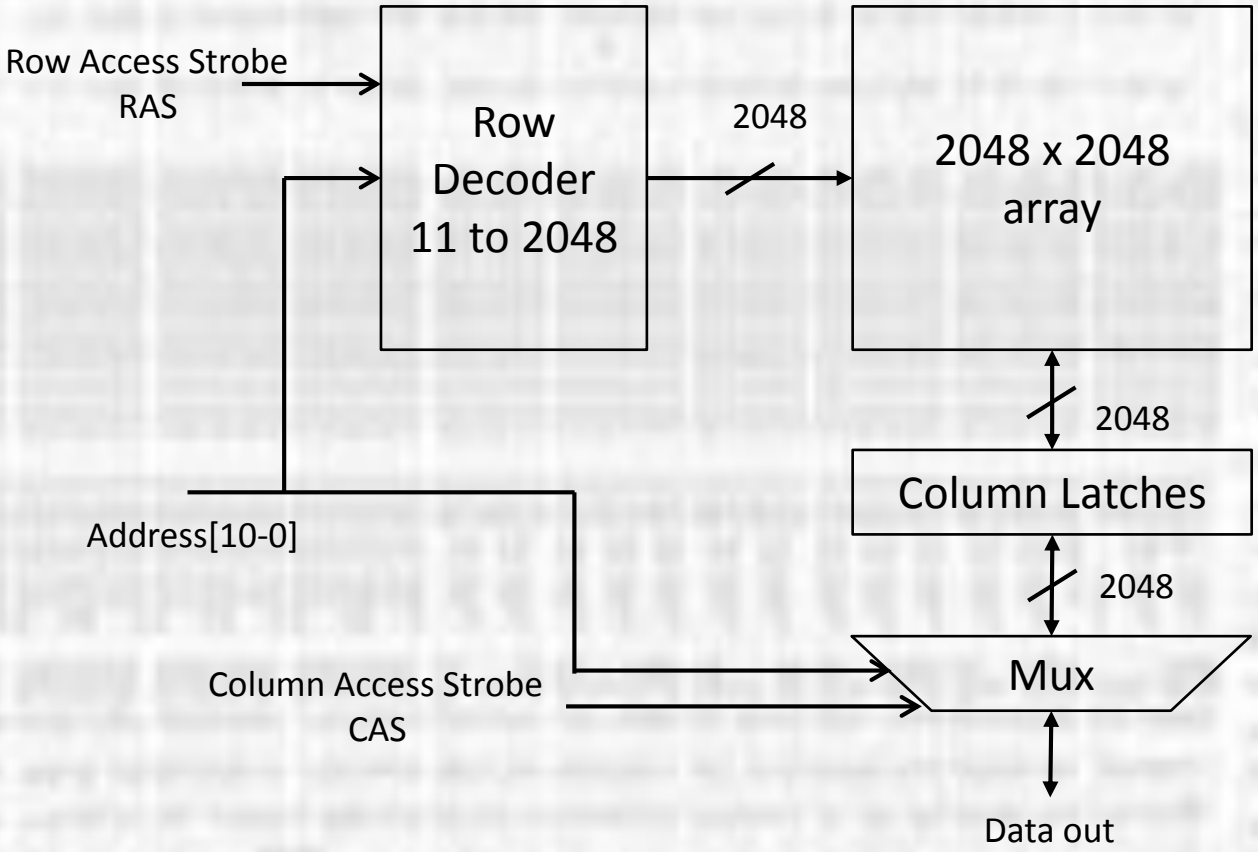
Memory Overview

Memory Types

- SDRAM
  - Array Layout – 4M X 1 DRAM



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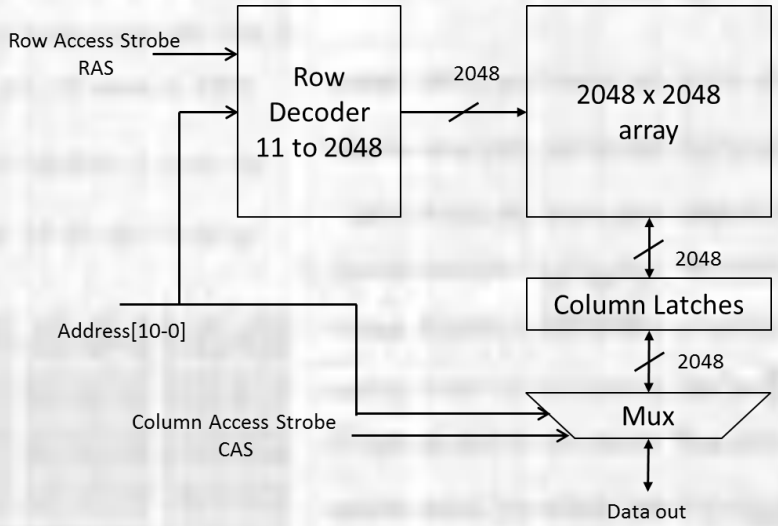
Memory Overview

Memory Types

- SDRAM
  - Random Access
  - 4M bits → 22 address bits
  - Operation
    - Place upper 11 bits on address bus
    - Strobe RAS
      - 2048 bits are latched
    - Place lower 11 bits on address bus
    - Strobe CAS
      - Selected bit is fed out



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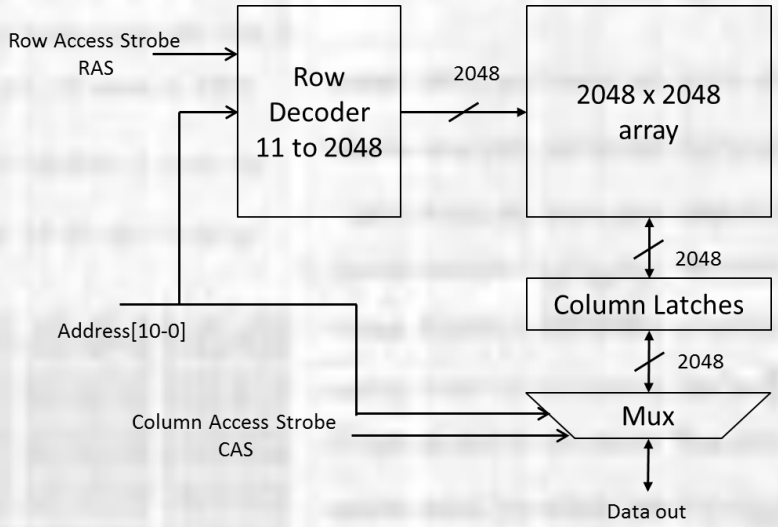
Memory Overview

Memory Types

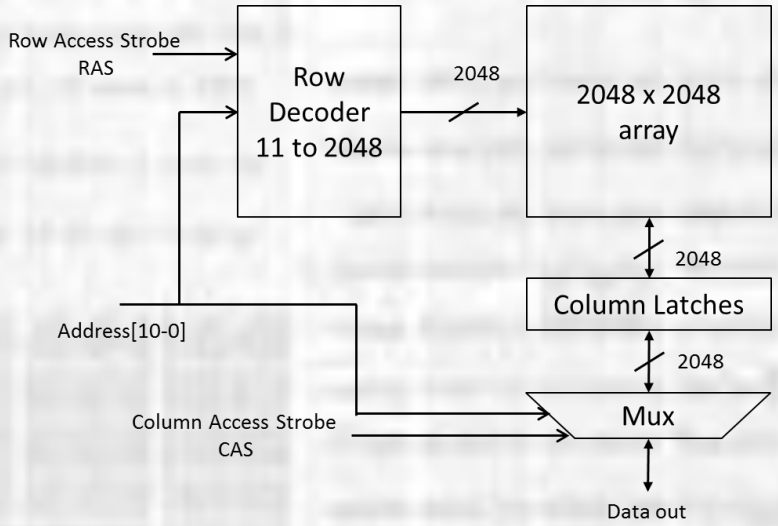
- SDRAM
  - Refresh
  - Operation
    - Controller selects a row address - Read
      - 2048 bits are latched
    - Same row address – Write
      - 2048 bits are refreshed



Memory Overview

Memory Types

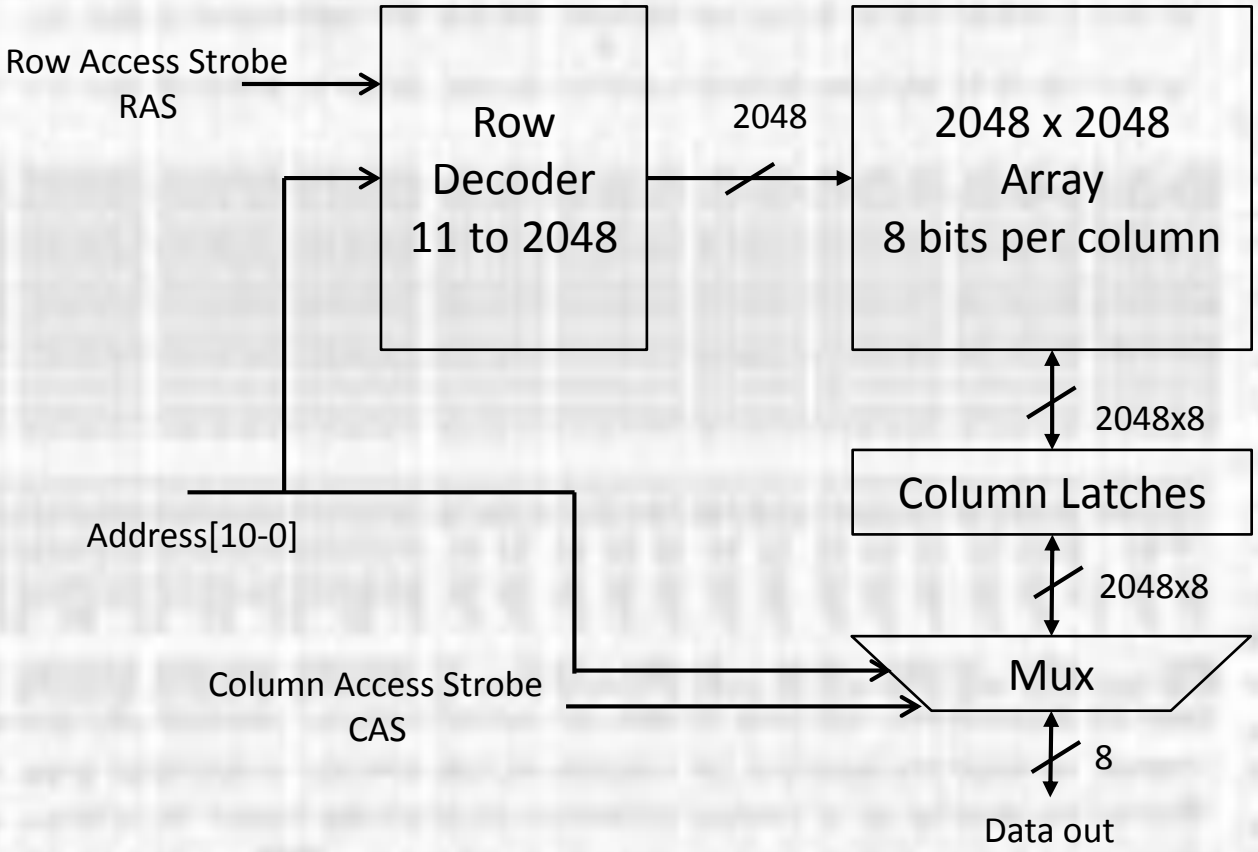
- SDRAM
  - Burst Operation
  - 4M bits → 22 address bits
  - Operation
    - Place upper 11 bits on address bus
    - Strobe RAS
      - 2048 bits are latched
    - Place lower 11 bits on address bus
    - Strobe CAS
      - Selected bit is fed out
    - Increment address latch
    - Next clock
      - Next bit is fed out
    - …



Memory Overview

Memory Types

- SDRAM
  - Array Layout – 4M X 8 DRAM



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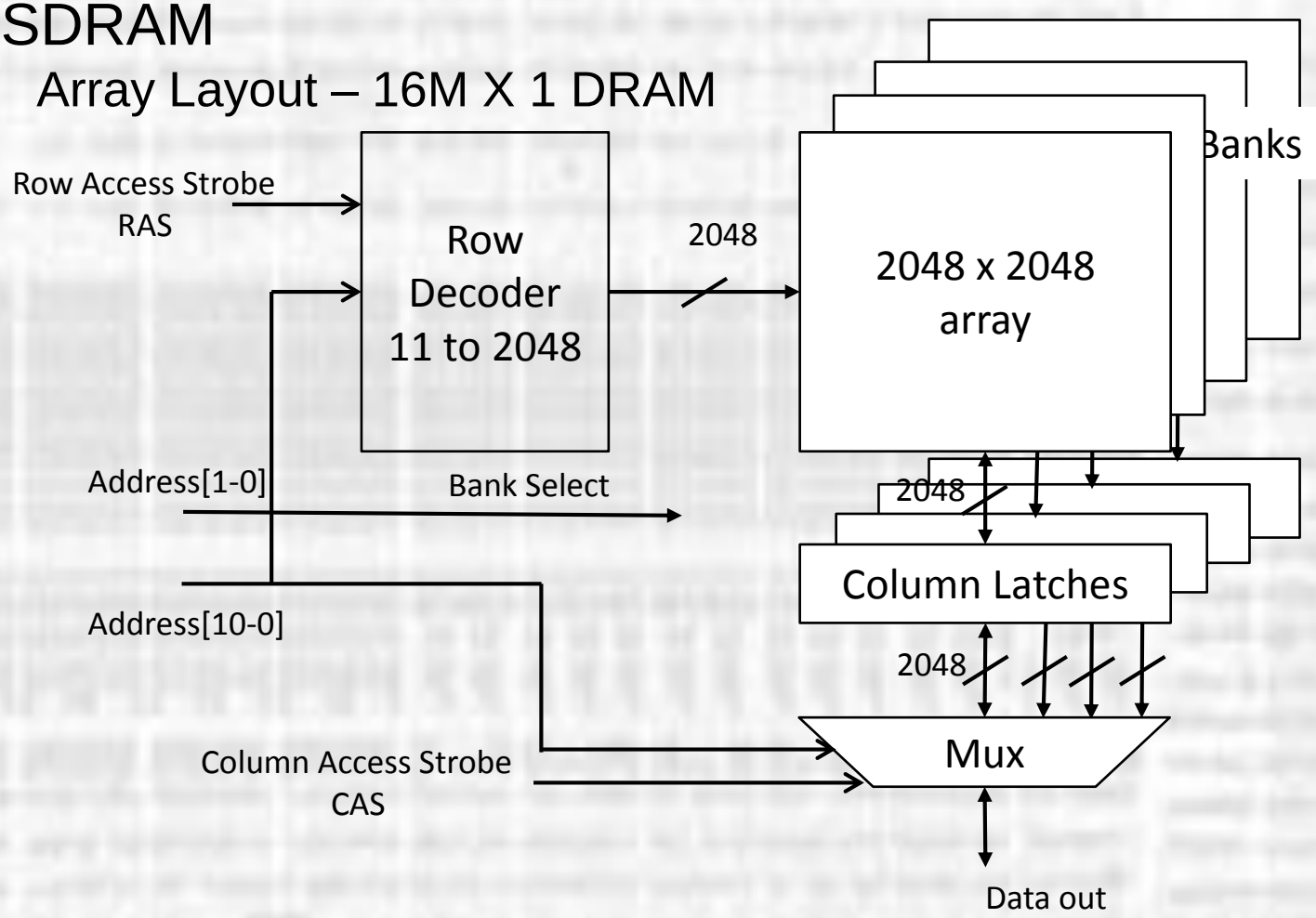
Memory Overview

Memory Types

- SDRAM
  - Array Layout – 16M X 1 DRAM



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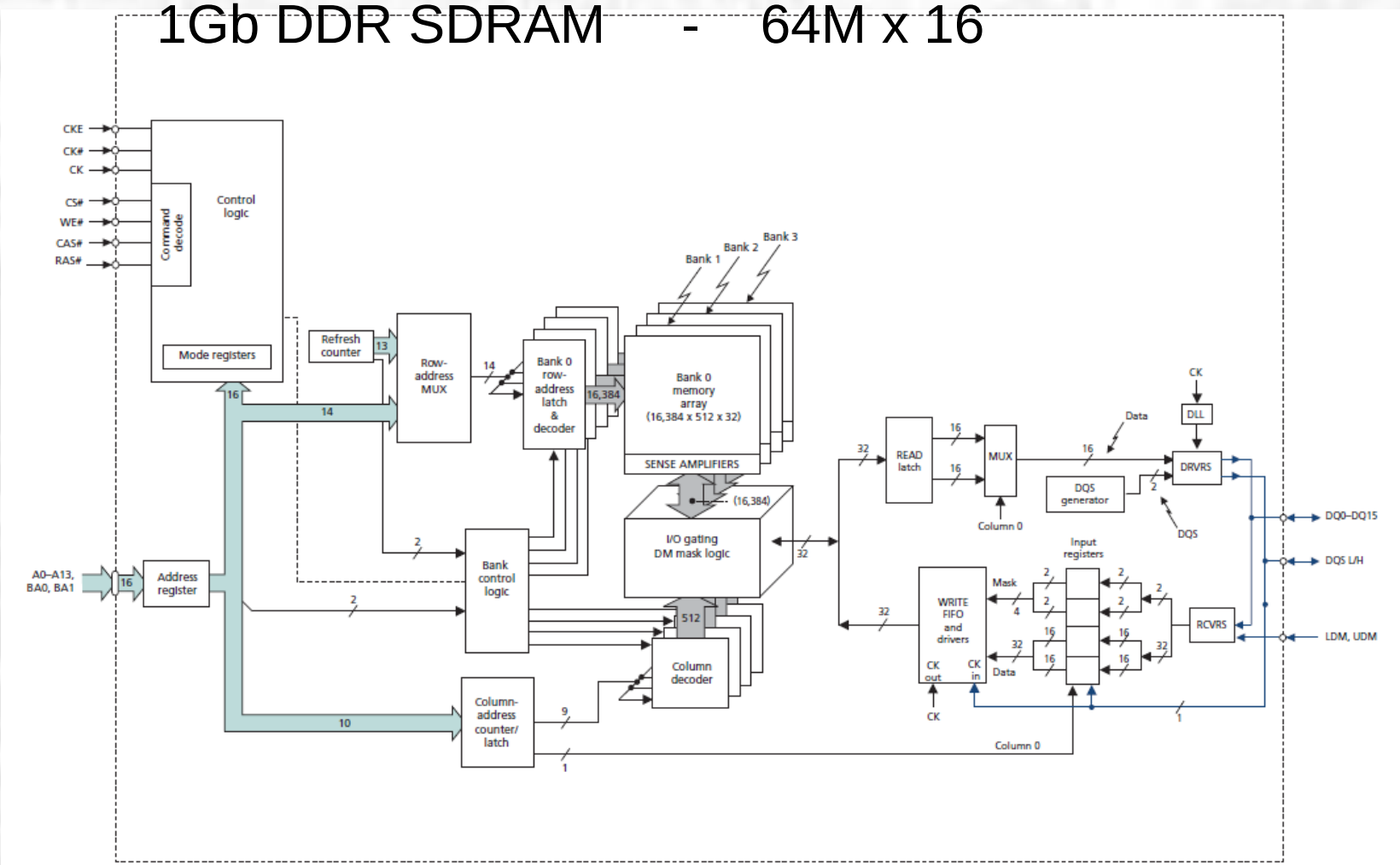
Memory Overview

Memory Types

1Gb DDR SDRAM - 64M x 16



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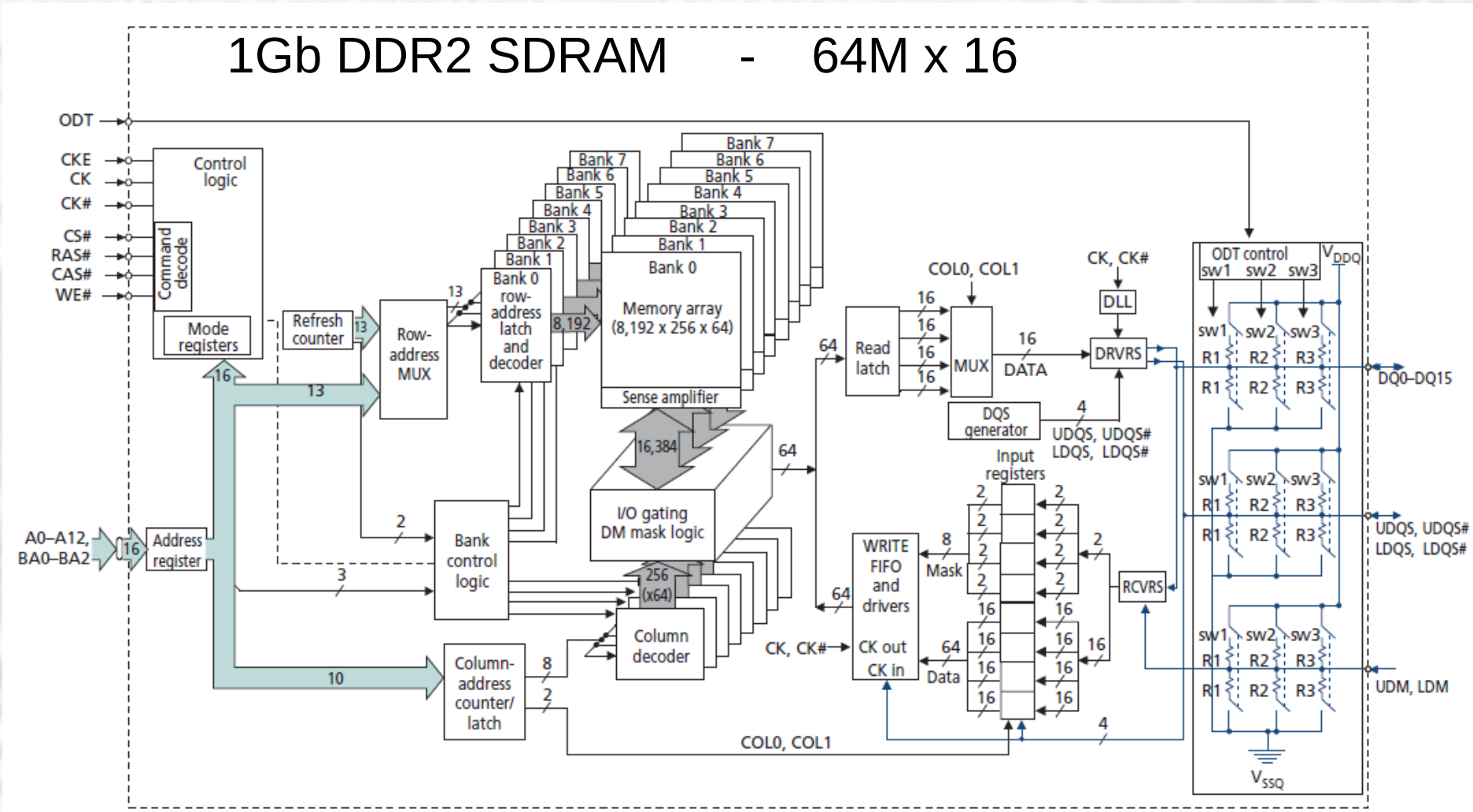
Memory Overview

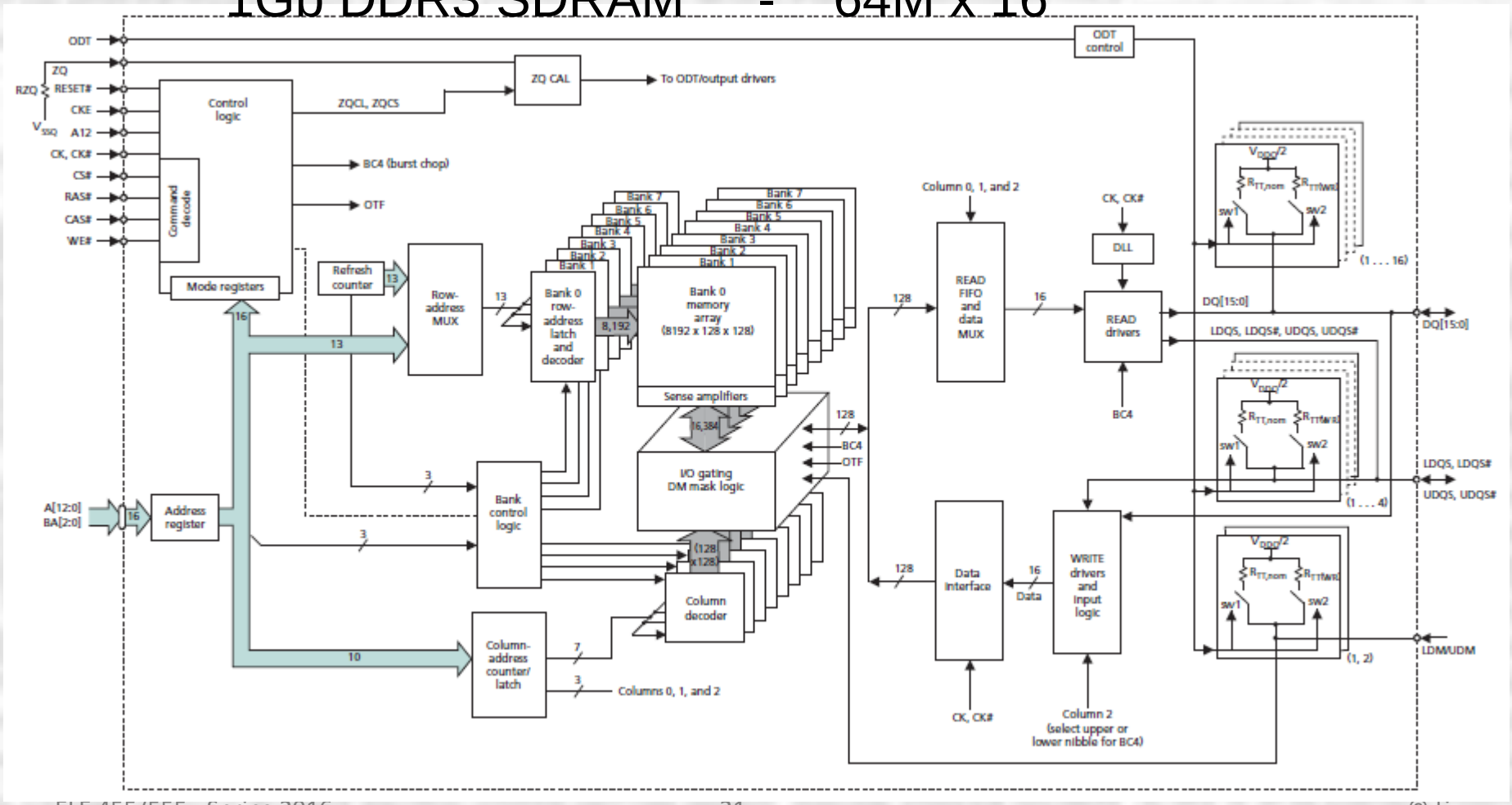
Memory Types



Memory Overview

Memory Types

1Gb DDR3 SDRAM - 64M x 16



Memory Overview

Memory Types

- SRAM
  - Latched (feedback) storage elements
    - Requires refresh
  - Static
    - As long as power is applied
  - Random Access
  - Row and Column access architecture
  - Synchronous
    - Allows additional bytes to be read/written on a single access

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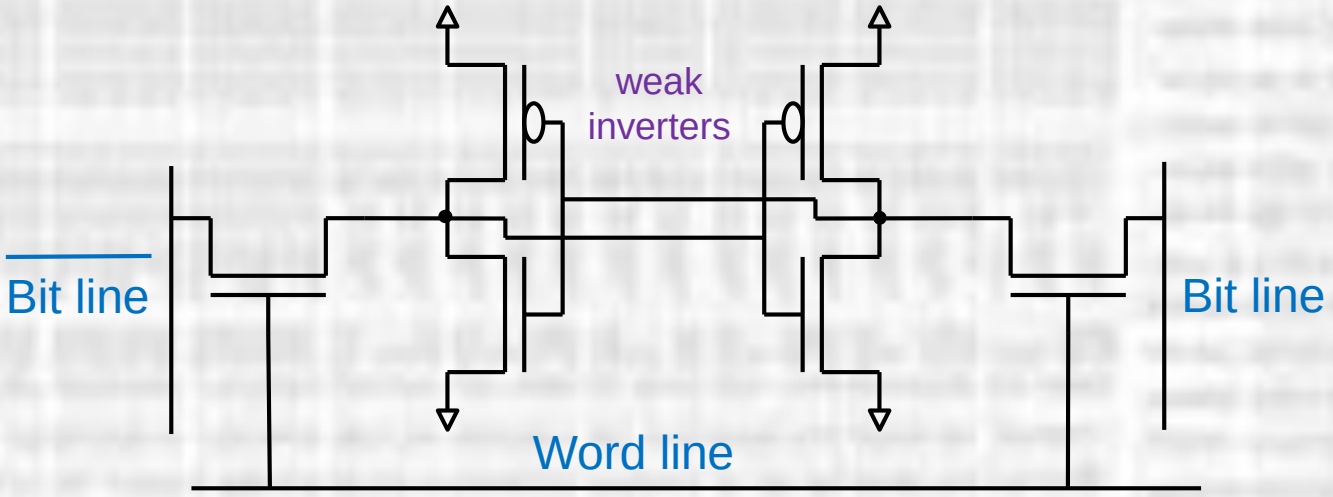
Memory Overview

Memory Types

- SRAM – Static Random Access Memory
  - Memory cell (1 bit) is based on a feedback circuit
  - Bit value is retained as long as power is maintained
  - Fastest read/write (R/W)
  - Highest power
  - Lowest density
  - Used in caches and small data memories



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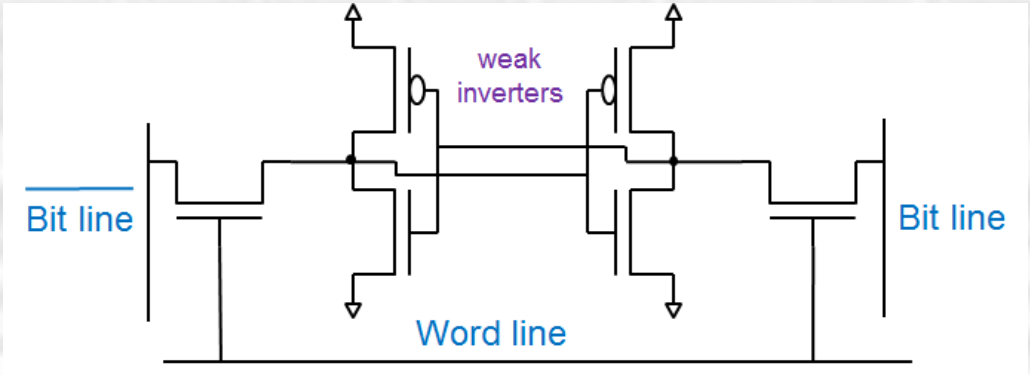
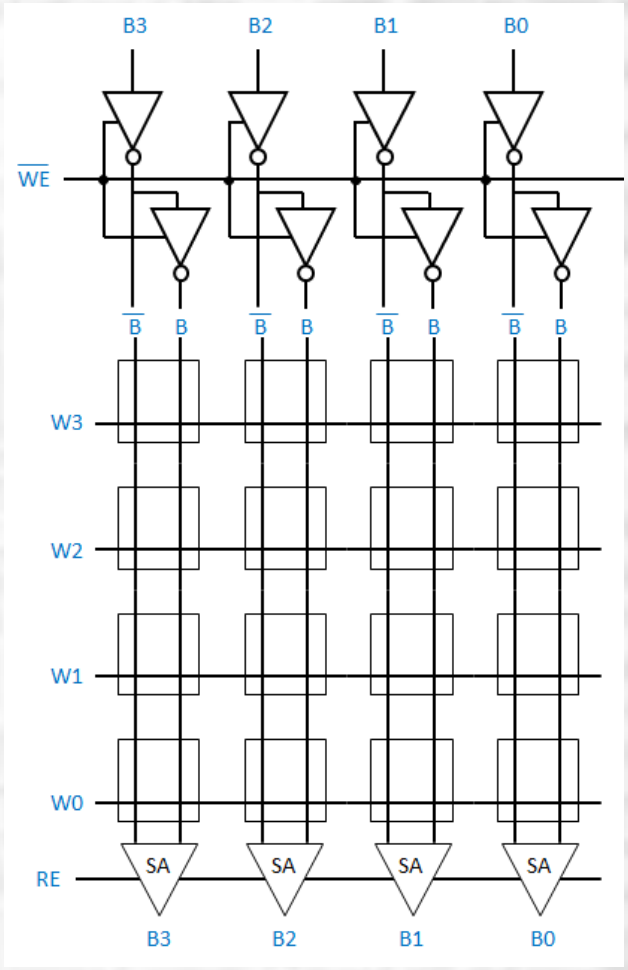
Memory Overview

Memory Types

- SRAM – Static Random Access Memory
  - Write
    - All Word lines low
    - Read Enable (RE) disabled (low)
    - Place B0, B1, B2, B3 on inputs
    - Pull write enable bar ($\overline{WE}$) low
    - Strobe the desired word line high
    - Bit lines override the bit cell inverters and store the new value in the cell





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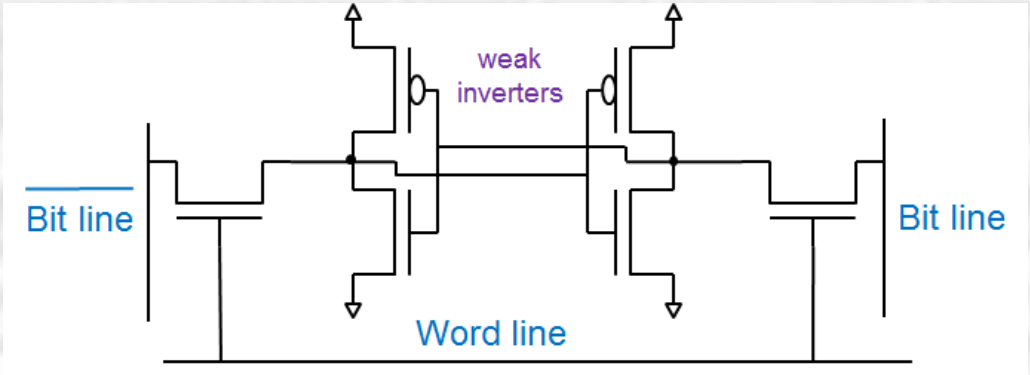
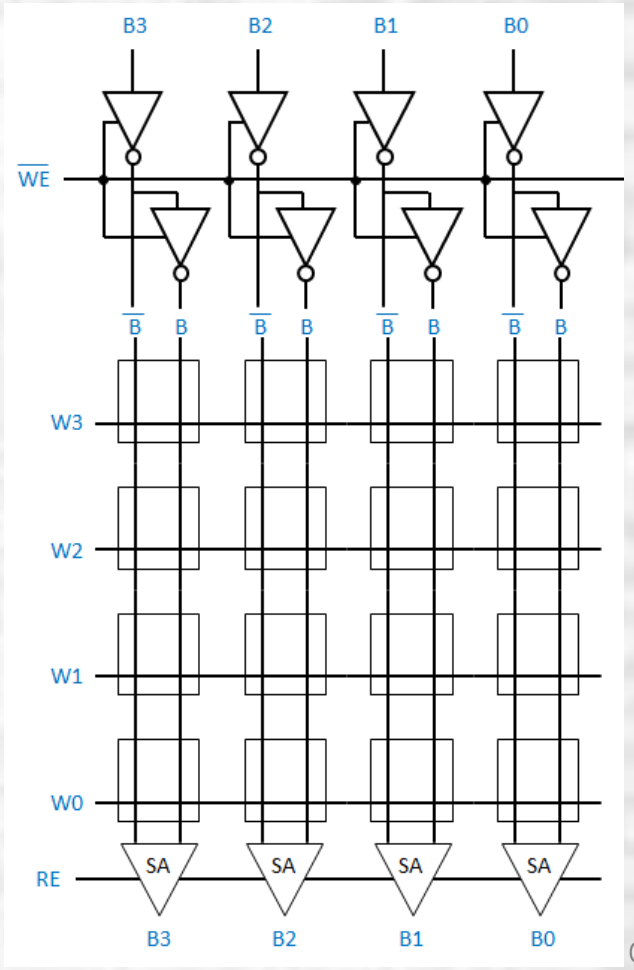
Memory Overview

Memory Types

- SRAM – Static Random Access Memory
  - Read
    - All Word lines low
    - Write enable bar ($\overline{WE}$) high
      - inverters tristated
    - Read Enable (RE) high
    - Strobe the desired word line high
    - Bit cell inverters drive the bit lines and sense amplifiers read the value





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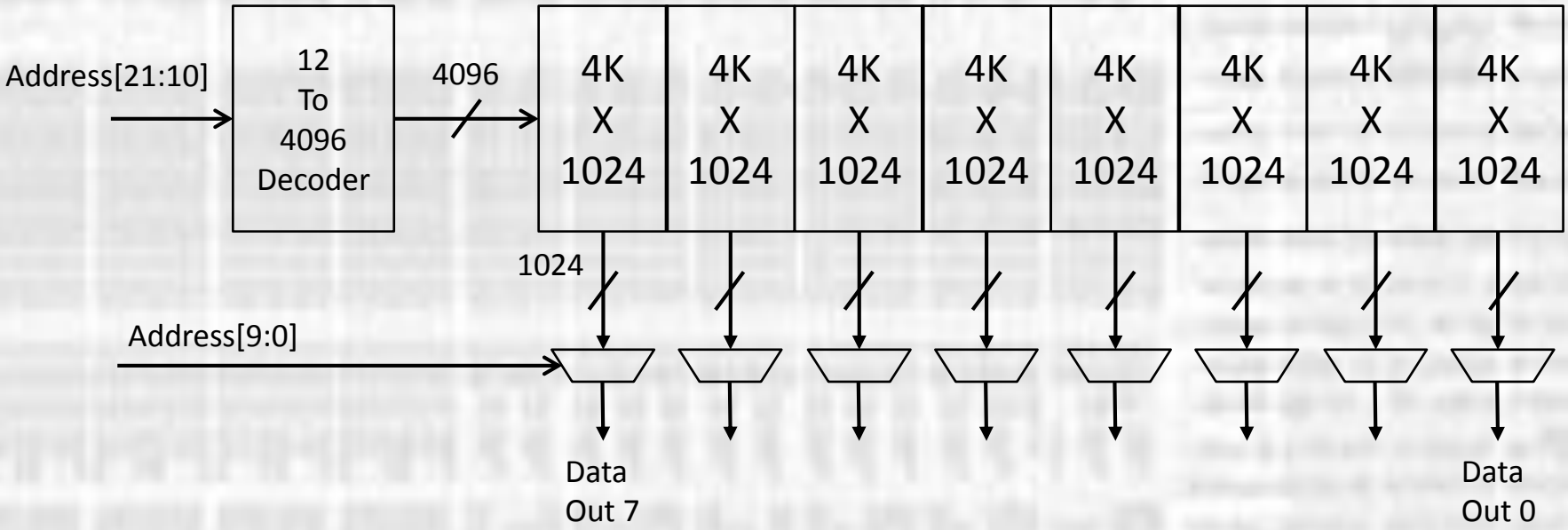
Memory Overview

Memory Types

- SRAM
  - Array Layout – 4M X 8



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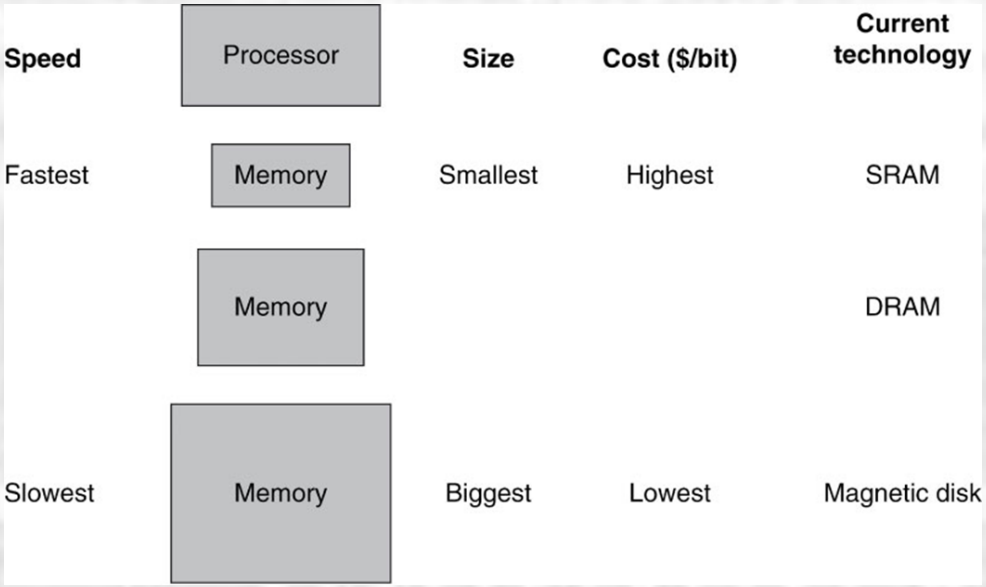
Memory Overview

Memory Types

- Memory Comparison



Technology	Typ Access Time	$/Gbyte (2012)
SRAM	0.5 - 2.5 ns	$500 - $1000
DRAM	50 - 70 ns	$10 - $20
Flash	5,000 - 50,000 ns	$0.75 - $2.00
Hard Disk	5,000,000 - 30,000,000 ns	$0.05 - $0.10

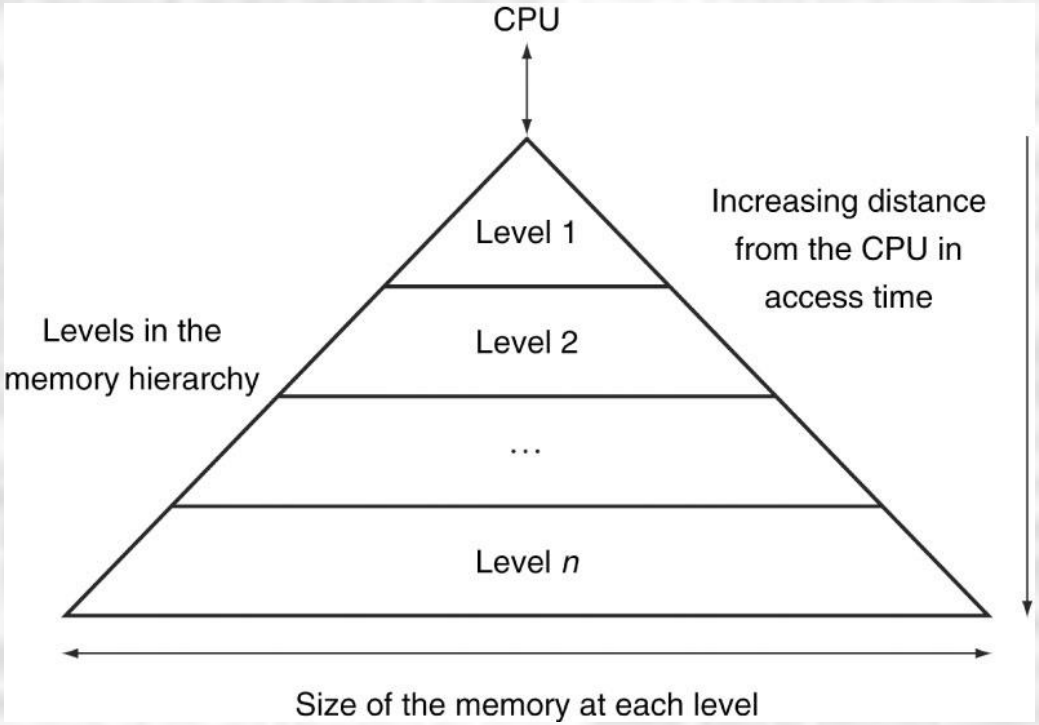
Memory Overview

Memory Hierarchy

- Critical Memory Considerations
  - Largest – slowest
  - Fastest – most expensive
  - Can't have everything in a single solution

→ **Memory Hierarchy**

  - Issue with a hierarchy
    - Must transfer data up and down the hierarchy
    - As slow as the slowest level addressed



Memory Overview

Memory Hierarchy

- Memory Hierarchy Considerations
  - Two aspects of processor applications make a memory hierarchy workable
    - Temporal Locality
      - You are more likely to uses something you recently used
        - Loops, calculated values, …
    - Spatial Locality
      - You are likely to use something that is close to something you recently used
        - Linear code, small loops, data structures

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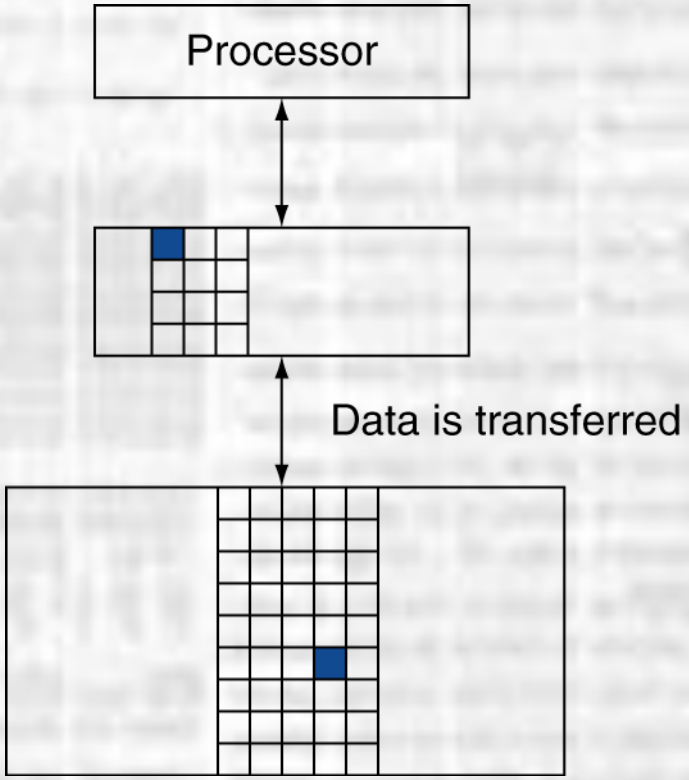
Memory Overview

Memory Hierarchy

- Memory Hierarchy Considerations
  - Transitions are limited between adjacent levels in the hierarchy
  - Transfer units of information
    - Line or Block
    - Different for each level
  - If what we want is in the memory we are looking at → HIT
  - If what we want is not in the memory we are looking at → MISS



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Memory Overview

Memory Hierarchy

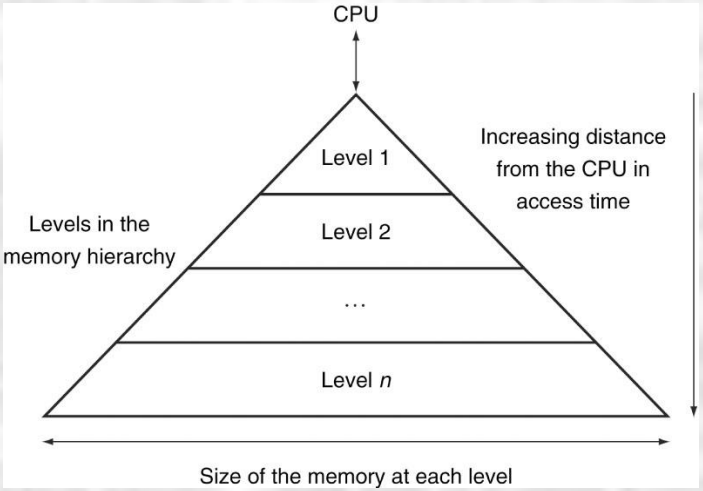
- Memory Hierarchy Considerations
  - Typical System

    Registers

    Cache (SRAM)

    Main Memory (DRAM)

    Storage (HDD or Flash)



  - Advanced systems may have 2,3,4 levels of cache
    - Each is progressively slower and larger
    - Size is targeted at holding entire applications

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