ELE 455/555 Computer System Engineering

Section 4 – Parallel Processing Class 1 – Challenges

- Motivation
 - Desire to provide more performance (processing)
 - Scaling a single processor is limited
 - Clock speeds
 - Power concerns
 - Cost (yield)
 - A group of multiple smaller processors used in parallel can resolve these concerns and provide additional flexibility
 - Requires effective software to succeed

- Perspective
 - Run multiple independent programs on a group of processors
 - Independent single-threaded applications

Task-level parallelism

• Single program running on a group of processors simultaneously

Parallel processing program

- Definitions
 - Multiple discrete processors

Clusters

- Multiple processors in a single chip
 - Individual processors are called Cores

Multi-Core Processor

These typically share a common physical memory

Shared Memory Processor (SMP)

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Definitions

- Software that performs in a linear fashion
 - Compiler, Motor Controller

Sequential Software

- Software that can handle multiple tasks in parallel
 - OS, Circuit Simulators

Concurrent Software

- Hardware / Software Compatibility
 - Need sequential software to run on both serial and parallel hardware
 - The challenge with parallel hardware is to try to utilize the resources
 - Need concurrent software to run on serial and parallel hardware
 - The challenge with serial hardware is performance
 - The challenge with parallel hardware is to utilize all the resources
 - # of parallel processors varies from system to system

		Sol	ftware
		Sequential	Concurrent
	Serial	Matrix Multiply written in MatLab running on an Intel Pentium 4	Windows Vista Operating System running on an Intel Pentium 4
Hardware	Parallel	Matrix Multiply written in MATLAB running on an Intel Core i7	Windows Vista Operating System running on an Intel Core i7

- It is difficult to create parallel processing programs
 - At the processor level (hardware) we have support via:
 - Sub-word parallelism
 - Superscalar hardware
 - Instruction level parallelism
 - Out-of-order, speculation
 - Cache coherence

- It is difficult to create parallel processing programs
 - We need to create EFFICIENT parallel processing programs
 - If the solution isn't efficient just use a single processor
 - If a single processor is not an option still need efficiencies to offset cost, power, complexity
 - Need: Faster, Lower Power

- It is difficult to create parallel processing programs
 - Many factors limit performance
 - Partitioning
 - · Need equal size tasks, otherwise parts of the system are waiting
 - Coordination
 - Synchronizing between processors to share data
 - Communications overhead
 - The actual time to communicate
 - Portions of the program that must be run sequentially

- It is difficult to create parallel processing programs
 - Example desire a 90x speedup using 100 processors what percentage of the program can be sequential

 $T_{new} = T_{parallelizable} / 100 + T_{sequential}$ Speedup = $\frac{1}{(1 - F_{parallelizable}) + F_{parallelizable} / 100} = 90$

Solving: F_{parallelizable} = 0.999

• Only 0.1% can be sequential

- It is difficult to create parallel processing programs
 - Example calculate 2 sums using 10 and 40 processors
 - a) 10 scalars must be sequential
 - b) 10 x 10 matrix parallelizable

```
If done entirely sequential
10 scalars = 10t 10x10 matrix = 100t total = 110t
```

Using 10 processors (only for the matrix) 10 scalars = 10t 10x10 matrix = 100t/10 = 10t total = 20t speed-up = 110t/20t = 5.5

Using 40 processors (only for the matrix) 10 scalars = 10t 10x10 matrix = 100t/40 = 2.5t total = 12.5t speed-up = 110t/12.5t = 8.8

• We quadrupled the number of processors and got less than 2x speed-up

- It is difficult to create parallel processing programs
 - Example calculate 2 sums using 10 and 40 processors
 - a) 10 scalars
 b) 20 x 20 matrix
 c) must be sequential
 c) parallelizable
 - If done entirely sequential 10 scalars = 10t 20x20 matrix = 400t total = 410t

Using 10 processors (only for the matrix) 10 scalars = 10t 20x20 matrix = 400t/10 = 40t total = 50t speed-up = 410t/50t = 8.2

Using 40 processors (only for the matrix) 10 scalars = 10t 20x20 matrix = 400t/40 = 10t total = 20t speed-up = 410t/20t = 20.5

We quadrupled the number of processors and got a little more than 2x speed-up

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- 2 ways to measure the speedup associated with a parallel processing solution
 - Strong Scaling
 - Keep the problem size fixed while increasing parallelism
 - Fixed customer base using a server farm
 - Faster streaming to customer base
 - Weak Scaling
 - Increase the problem size with increasing parallelism
 - ATM processing central office
 - More customers, not more ATM transactions per customer

- Scaling Example strong
 - calculate 2 sums using 10 and 100 processors
 - a) 10 scalars
 b) 10 x 10 matrix
 c) must be sequential
 c) parallelizable

```
If done entirely sequential
10 scalars = 10t 10x10 matrix = 100t total = 110t
```

Using 10 processors (only for the matrix) 10 scalars = 10t 10x10 matrix = 100t/10 = 10t total = 20t speed-up = 110t/20t = 5.5

Using 100 processors (only for the matrix) 10 scalars = 10t 10x10 matrix = 100t/100 = 1t total = 11t speed-up = 110t/11t = 10

- We achieved 55% of the potential for 10 processors
- We achieved 10% of the potential for 100 processors

- Scaling Example weak (100x100 matrix)
 - calculate 2 sums using 10 and 100 processors

 a) 10 scalars
 b) 100 x 100 matrix
 parallelizable

If done entirely sequential 10 scalars = 10t 100x100 matrix = 10,000t total = 10,010t

Using 10 processors (only for the matrix) 10 scalars = 10t 100x100 matrix = 10,000t/10 = 1000t total = 1010t speed-up = 10010t/1010t = 9.9

Using 100 processors (only for the matrix) 10 scalars = 10t 100x100 matrix = 10,000t/100 = 100t total = 110t speed-up = 10,010t/110t = 91

- We achieved 99% of the potential for 10 processors
- We achieved 91% of the potential for 100 processors

- Balance Example
 - Example calculate 2 sums using 40 processors
 - a) 10 scalars must be sequential
 - b) 20 x 20 matrix parallelizable

AND – force 1 parallel processor to carry 2x and 5x the normal load

Using 40 processors (only for the matrix) and a balanced load 10 scalars = 10t 20x20 matrix = 400t/40 = 10t total = 20t speed-up = 410t/20t = 20.5

With unbalanced load of 2x, remaining processor sit idle so just look at this case 10 scalars = 10t 20x20 matrix = max[20t/1, 380t/39] = 20t total = 30t speed-up = 410t/30t = 14

With unbalanced load of 5x, remaining processor sit idle so just look at this case 10 scalars = 10t 20x20 matrix = max[50t/1, 350t/39] = 50t total = 60t speed-up = 410t/60t = 7

• The unbalanced load significantly limits the performance improvement

4 Basic Instruction / Data Configurations

	1000 44	Data Streams		
		Single	Multiple	
Instruction Streams	Single	SISD: Intel Pentium 4	SIMD: SSE instructions of x86	
	Multiple	MISD: No examples today	MIMD: Intel Xeon e5345	

• MIMD

 While we could spread multiple programs across multiple processors in a MIMD system
 the usual case is to spread a single program's instructions across multiple processors

Single Program Multiple Data (SPMD)

- Typical application for MIMD
- Use conditional statements to spread portions of the program to various processors
- May need a copy of the code for each processor

Parallel Process Instruction/Data Are

• MIMD

 While we could spread processors in a MIMD program's instructions

Single Program Multipl

- Typical application for M
- Use conditional statem various processors
- May need a copy of the

	Processes 15	76 CPO US	age
883	Image	PID	Descrip
oto Ari	ccSvcHst.exe	2836	Symant
	dwm.exe	6040	Deskto
6 L 1 E E	WmiPrvSE.exe	4500	WMI Pr
	svchost.exe (netsvcs)	1048	Host Pr
	Smc.exe	4868	Symant
	ccSvcHst.exe	5980	Symant
	svchost.exe (LocalServiceAn	1748	Host Pr
	svchost.exe (LocalSystemNet	516	Host Pr
	HostedAgent.exe	3868	Hosted

Service: Name

SepMast

LanmanS

SmcServi

SysMain

iphlpsvc

SSDPSRV

ProfSvc

niSvcLoc

WSearch

Image

Nesource Monitor

Overview CPU

Memory Disk

Smc.exe	4868	Symant	Runni	31	0	0.01
ccSvcHst.exe	5980	Symant	Runni	20	0	0.01
svchost.exe (LocalServiceAn	1748	Host Pr	Runni	16	0	0.01
svchost.exe (LocalSystemNet	516	Host Pr	Runni	21	0	0.01
HostedAgent.exe	3868	Hosted	Runni	30	0	0.01
taskmgr.exe	4428	Windo	Runni	7	0	0.01
chrome.exe	7176	Googl	Runni	10	0	0.01
Isass.exe	824	Local S	Runni	11	0	0.01
googledrivesync.exe	7152	Googl	Runni	27	0	0.01
SearchIndexer.exe	1304	Micros	Runni	15	0	0.00
POWERPNT.EXE	9008	Micros	Runni	14	0	0.00
chrome.exe	7124	Googl	Runni	37	0	0.00
SystemWebServer.exe	2528	System	Runni	32	0	0.00
svchost.exe (LocalServiceNet	632	Host Pr	Runni	19	0	0.00
svchost.exe (RPCSS)	484	Host Pr	Runni	10	0	0.00

Superf...

IP Helper

SSDP D...

User Pr...

NI Syst...

Windo...

Type

Select a process or search handles to see results.

Runni...

Runni...

Runni...

Runni...

Runni...

Runni...

LocalS...

NetSvcs

LocalS...

netsycs

Search Handles

Handle Name

Network

Status

Runni...

Runni...

Runni...

Runni...

105% Maximum Frequency

Threads

72

5

11

45

CPU

0

0

0

0

CPU

0

0

0

0

0

0

0

0

0

s 📕 0	% CPU Us	age	_	_
	PID	Descrip	Status	Group
erService	2836	Symant	Runni	
erver	1048	Server	Runni	netsvcs
ce	4868	Symant	Runni	

516

1048

1748

1048

2528

1304

PID



~

Averag...

0.18

0.05

0.04

0.04

~

Averag...

0.12

0.02

0.01

0.01

0.01

0.01

0.01

0.00

0.00

P 44 (A

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CPU 7 - Parked

Associated Modules

Associated Handles

 \sim

SIMD

- Very much like SISD
 - Execution of a single instruction across multiple processors using vector data
 - One PC, n register sets
 - Program looks just like a sequential program
 - One copy of the code

- Vector Architecture
 - Old days array of processors
 - Now large register set feeding a pipelined execution unit
 - e.g. 32 vector registers, each with 64, 64bit words
 - Reduces overhead code
 - loops reduced
 - Reduces potential hazards
 - Reduces fetch bandwidth
 - Reduces data bandwidth
 - Data with-in a vector must be independent

- Vector Architecture
 - Y = (a x X) + Y
- Conventional MIPS code 1.d \$f0,a(\$sp) ;load scalar a ;upper bound of what to load addiu r4,\$s0,#512 loop: l.d \$f2,0(\$s0) ; load x(i)mul.d \$f2,\$f2,\$f0 ; $a \times x(i)$ 1.d \$f4_0(\$<u>s</u>1) ; load y(i)add.d \$f4,\$f2 ; $a \times x(i) + y(i)$ s.d \$f4,0(\$s1) ;store into y(i) addiu \$s0,\$s0,#8 ; increment index to x addiu \$s1,\$s1,#8 ; increment index to y subu \$t0,r4,\$s0 ;compute bound bne \$t0,\$zero,loop ;check if done

- Vector Architecture
 - Y = (a x X) + Y
 - Vector MIPS code

1.d	\$f0,a(\$sp)
1v	\$v1,0(\$s0)
mulvs.d	\$v2,\$v1,\$f0
1v	\$v3,0(\$s1)
addv.d	\$v4,\$v2,\$v3
sv	\$v4,0(\$s1)

;load scalar a
;load vector x
;vector-scalar multiply
;load vector y
;add y to product
;store the result

- Vector Architecture
 - Strided Access
 - · Read every nth element from memory to place in the vector register
 - Replaces a n iteration loop
 - Gather-scatter
 - Read the vector values from around the memory (gather)
 - Store the results around the memory (scatter)

- Vector Architecture
 - Lanes
 - Parallel combinations of vector pipelines





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- Vector Architecture
 - Lanes
 - Parallel combinations of vector pipelines

