ELE 655
Microprocessor System Design

Section 4 – Thread Level Parallelism

Class 2 – AXI Introduction

Parallel Communications

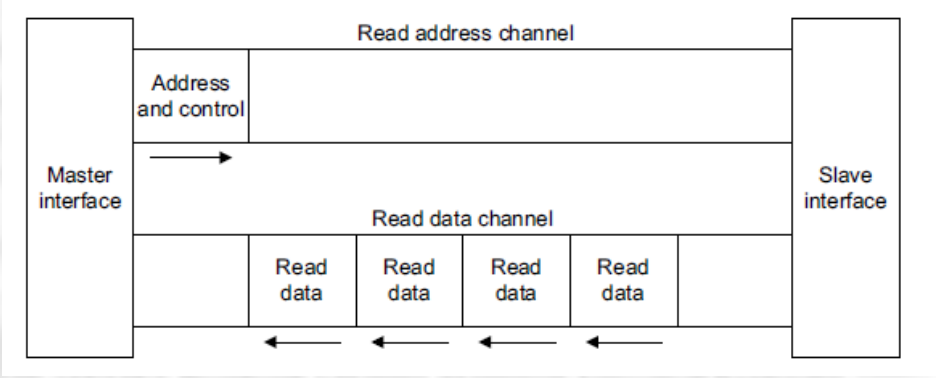
On-chip Bus Structures

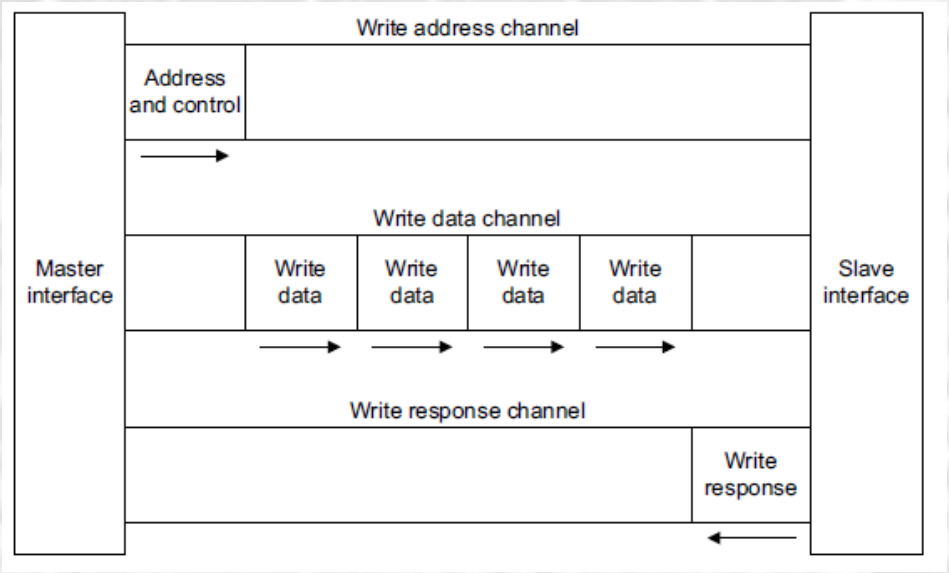
- AMBA – AXI
  - Advanced eXtensible Interface
  - Burst based protocol
  - 5 independent transaction channels
    - Read address
    - Read data
    - Write address
    - Write data
    - Write response

Parallel Communications

On-chip Bus Structures

- AMBA – AXI

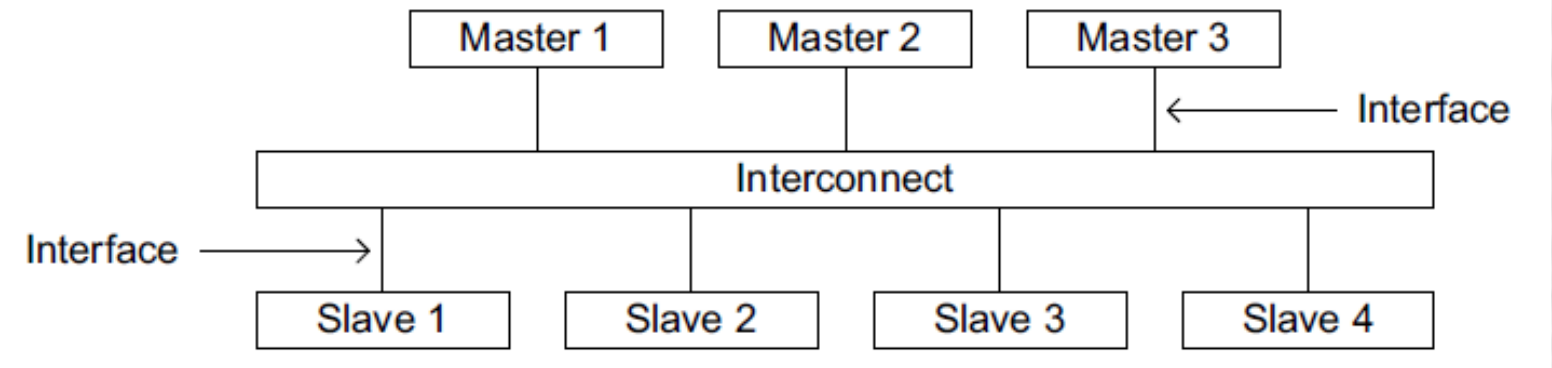




Parallel Communications

On-chip Bus Structures

- AMBA – AXI interface
  - Interfaces defined between
    - Master and interconnect
    - Slave and Interconnect
    - Master and Slave
  - The Interconnect is implementation specific



Parallel Communications

On-chip Bus Structures

- AMBA – AXI system topologies
  - Three common interconnect topologies
    - Shared address and data buses
    - Shared address buses and multiple data buses
    - Multilayer - multiple address and data buses.
  - In most systems
    - Address channel bandwidth requirement is significantly less than data channel bandwidth requirement
    - Use a shared address bus with multiple data buses
      - Enable parallel data transfers
      - Balance between system performance and interconnect complexity

Parallel Communications

On-chip Bus Structures

- AMBA – AXI system topologies
  - All channels are unidirectional
  - All channels are independent
    - No fixed timing requirement between channels
  - Allows for Register Slice insertion
    - Add registers into the channels to increase clock speeds
    - Cost is increased latencies
    - Provides a good solution for a mix of short and long paths

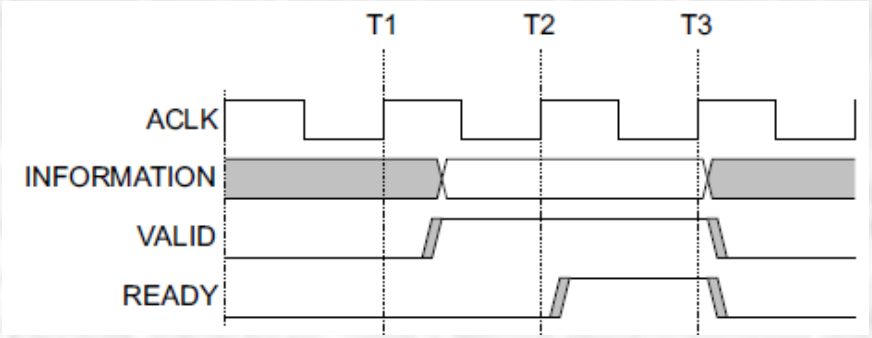
Parallel Communications

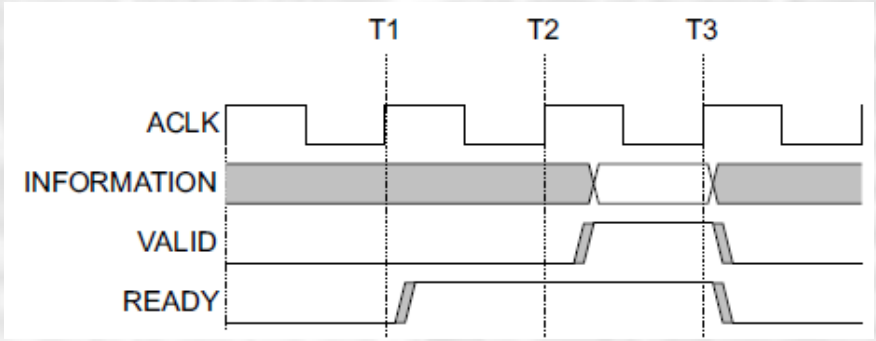
On-chip Bus Structures

- AMBA – AXI Signaling
  - All 5 channels use a handshake process to ensure proper communication
  - Either source or destination can control rate of transfer
    - CLK
    - VALID – generated by the source
    - READY – Generated by the destination
    - Information can be address, data, control

Transaction channel	Handshake pair
Write address channel	AWVALID, AWREADY
Write data channel	WVALID, WREADY
Write response channel	BVALID, BREADY
Read address channel	ARVALID, ARREADY
Read data channel	RVALID, RREADY

    - Transactions occurs on rising CLK edge with both VALID and READY high





Parallel Communications

On-chip Bus Structures

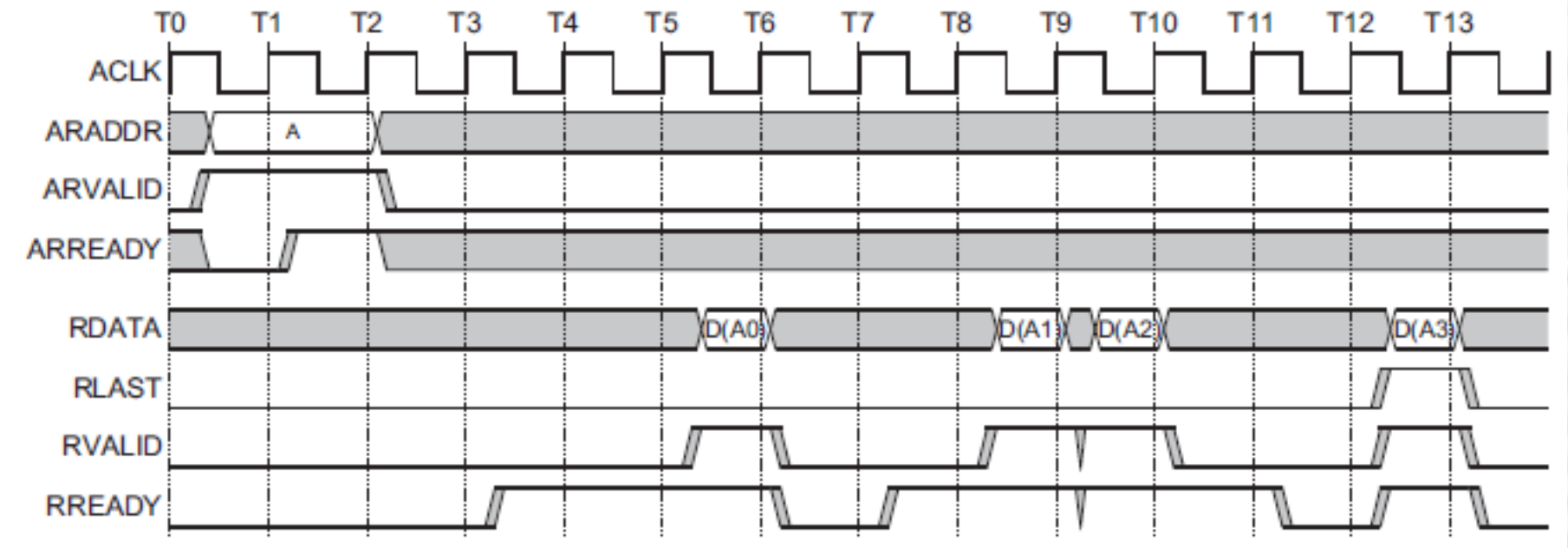
- AMBA – AXI Signaling
  - Source – Destination ≠ Master – Slave
  - Master = processor
  - Slave = memory or peripheral
  - Source = origin of information
  - Destination = recipient of information
  - Read
    - Master = Processor, Slave = Memory
    - Control and address: Source = Processor, Destination = Memory
    - Data: Source = Memory, Destination = Processor
  - Write
    - Master = Processor, Slave = Memory
    - Control and address: Source = Processor, Destination = Memory
    - Data: Source = Processor, Destination = Memory

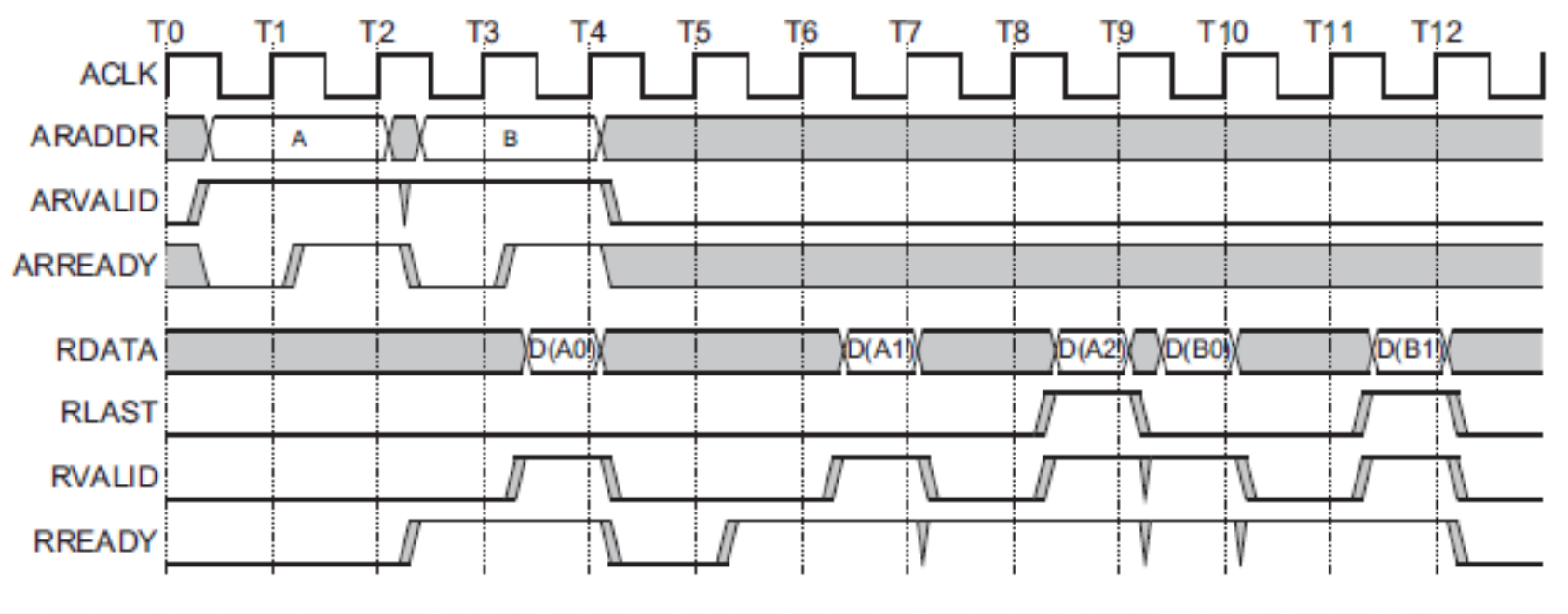
Parallel Communications

On-chip Bus Structures

- AMBA – AXI Signaling
  - Transactions are burst oriented
    - Beat - increment of data transfer – (# bytes in a word)
    - Burst – series of transfers in a fixed configuration
    - Master drives Control and Address of first byte location to Slave
    - Slave is responsible for calculating subsequent addresses for the transfer

** Bursts are not allowed to cross 4KB boundaries
This is also the minimum address space for a slave


T0
T1
T2
T3
T4
T5
T6
T7
T8
T9
T10
T11
T12
T13
ACLK
ARADDR
A
ARVALID
ARREADY
RDATA
D(A0)
D(A1)
D(A2)
D(A3)
RLAST
RVALID
RREADY


T0
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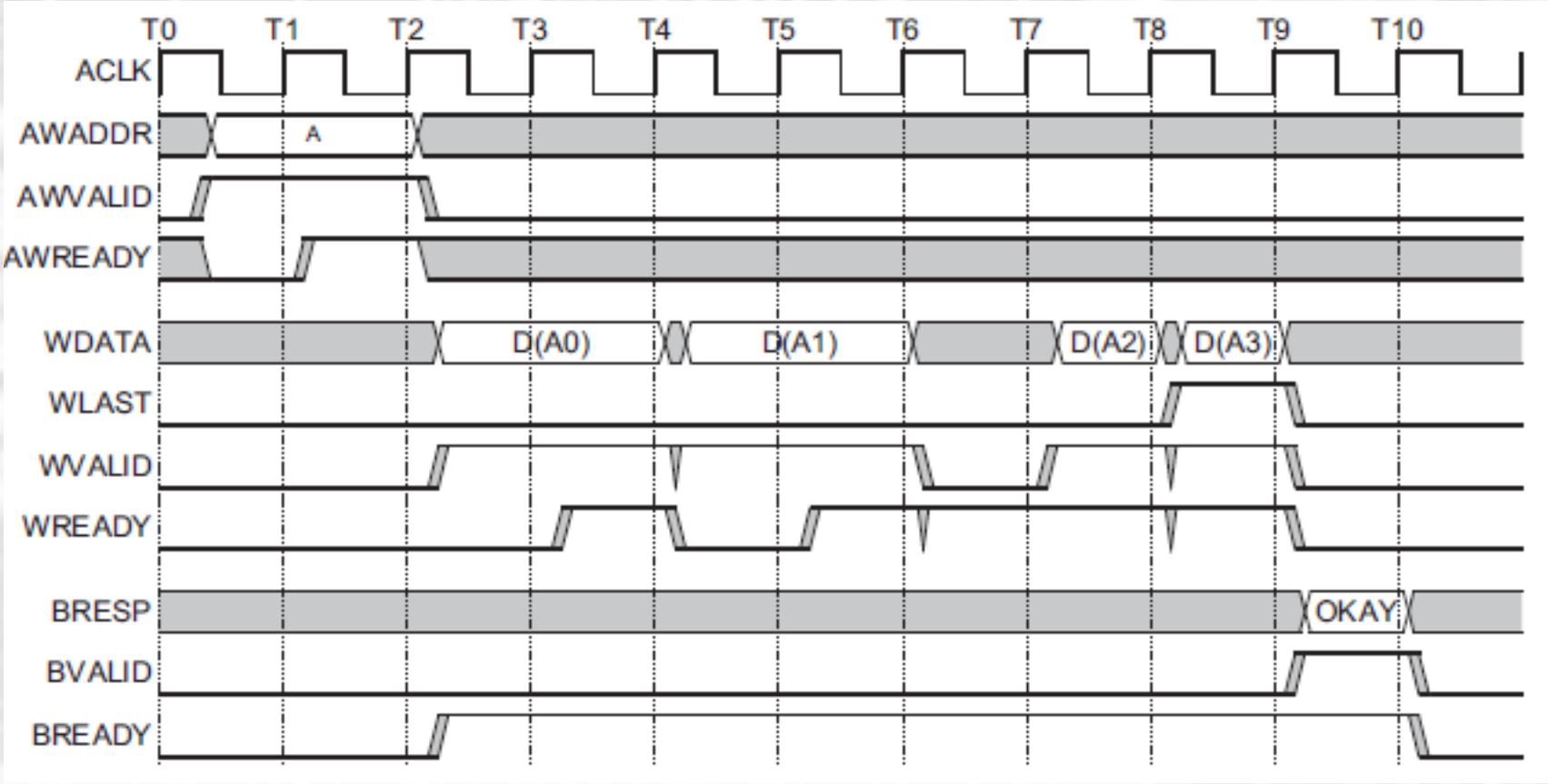
T11
T12
ACLK
ARADDR
A
B
ARVALID
ARREADY
RDATA
D(A0)
D(A1)
D(A2)
D(B0)
D(B1)
RLAST
RVALID
RREADY


T0
T1
T2
T3
T4
T5
T6
T7
T8
T9
T10
ACLK
AWADDR
A
AWVALID
AWREADY
WDATA
D(A0)
D(A1)
D(A2)
D(A3)
WLAST
WVALID
WREADY
BRESP
OKAY
BVALID
BREADY

Parallel Communications

On-chip Bus Structures

- AMBA – AXI Signaling - Address
  - Address – physical addressing
    - Signals to indicate desired R/W address
    - Supports 32, 40, 44 and 48 bit addressing
    - AxADDR[n:0]
      - n = 32,40,44 or 48

ARADDR[ ] - Address channel Read Address
AWADDR[ ] - Address channel Write Address
AxADDR[ ] - Address channel Address – applies to both R/W

Parallel Communications

On-chip Bus Structures

- AMBA – AXI Signaling - Control
  - Beat Size (Burst Size) - increment of data transfer
    - # of bytes transferred in each transaction
    - Sizes from 1-128 bytes supported
      - 64 bit processor would use 8 byte beat size
      - Could hardwire bits if this never changed
    - Specified by signals on Address Read and Address Write Channels
    - AxSize[2:0]

** ARM calls this the Burst Size

ARSIZE[ ] - Address channel Read burst Size
AWSIZE[ ] - Address channel Write burst Size
AxSIZE[ ] - Address channel burst Size– applies to both R/W

AxSIZE[2:0]	Bytes in transfer
0b000	1
0b001	2
0b010	4
0b011	8
0b100	16
0b101	32
0b110	64
0b111	128

Parallel Communications

On-chip Bus Structures

- AMBA – AXI Signaling - Control
  - Burst Length – number of Beats in a Burst
    - # of Beats transferred in each Burst
    - Sizes from 1 - 256 Beats supported
    - Specified by signals on Address Read and Address Write Channels
    - AxLEN[7:0]
      - Length = AxLEN[7:0] + 1

** Lengths > 16 only allowed in INCR mode

Parallel Communications

On-chip Bus Structures

- AMBA – AXI Signaling - Control
  - Burst Type – Type of Burst
    - Fixed – same address used for each Beat of the Burst
      - Typical for R/W to a FIFO
    - Incremental – address is incremented (by Slave) by Beat size for each Beat in the Burst
      - Typical for accessing sequential memory
    - Wrapping – Incremental burst with boundary wrapping
      - 4 byte beat, 8 beat burst, starting address 0x08
      - Burst would access addresses 0x08, 0x0C, 0x10, 0x14, 0x18, 0x1C, 0x00, 0x04
      - Starting address must be Beat aligned
      - Burst lengths of 2,4,8 and 16 allowed
    - AxBURST[1:0]

AxBURST[1:0]	Burst type
0b00	FIXED
0b01	INCR
0b10	WRAP
0b11	Reserved

Parallel Communications

On-chip Bus Structures

- AMBA – AXI Signaling - Control
  - Additional Controls
    - AxCACHE[3:0]
      - Bufferable – Data (W) may be buffered prior to reaching final destination
      - Modifiable –
        - Data may be allocated to a location other than the final destination
        - Transactions can be re-ordered
        - Transaction controls can be modified
      - Allocation – Indicates Data was allocated previously
    - AxPROT[2:0]
      - Indicates access protection to memory locations

AxCACHE	Value	Transaction attribute
[0]	0	Non-bufferable
	1	Bufferable
[1]	0	Non- modifiable
	1	modifiable
[2]	0	No Read-allocate
	1	Read-allocate
[3]	0	No Write-allocate
	1	Write-allocate

AxPROT	Value	Function
[0]	0	Unprivileged access
	1	Privileged access
[1]	0	Secure access
	1	Non-secure access
[2]	0	Data access
	1	Instruction access

Parallel Communications

On-chip Bus Structures

- AMBA – AXI Signaling - Data
  - Data – implementation specific
    - Read or Write date
    - Typically 32, 64, 128 bits wide
    - Relationship between Data width and Beat Size
    - xDATA[n:0]
      - n = 32,64,128,…

RDATA[ ] - Read Data
WDATA[ ] - Write Data

Parallel Communications

On-chip Bus Structures

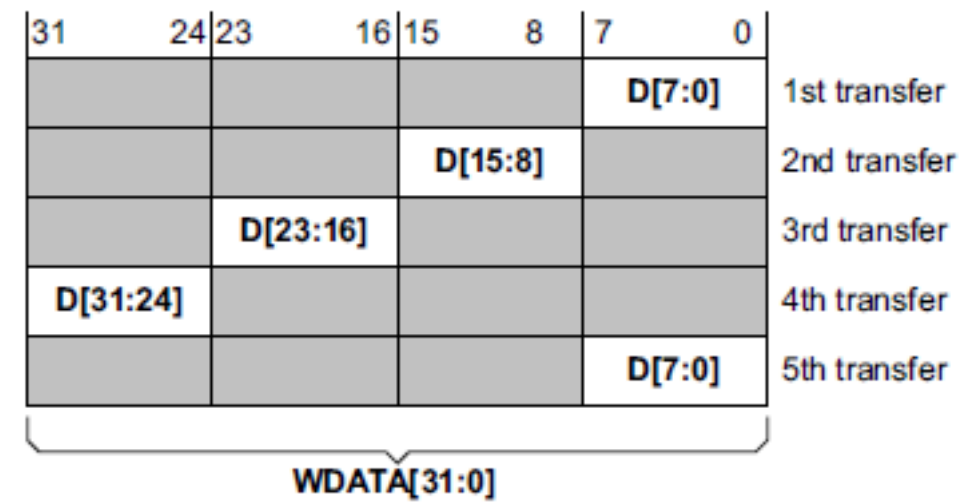
- AMBA – AXI Signaling - Data
  - Last – indicates the last transfer in a burst
    - RLAST – Read channel Last signal
      - generated by slave
    - WLAST – Write channel last signal
      - generated by the master

Parallel Communications

On-chip Bus Structures

- AMBA – AXI Signaling - Data
  - Relationship between Data width and Beat Size
    - 1 Byte Beat
    - 5 Beat Burst
    - 32 bit data bus

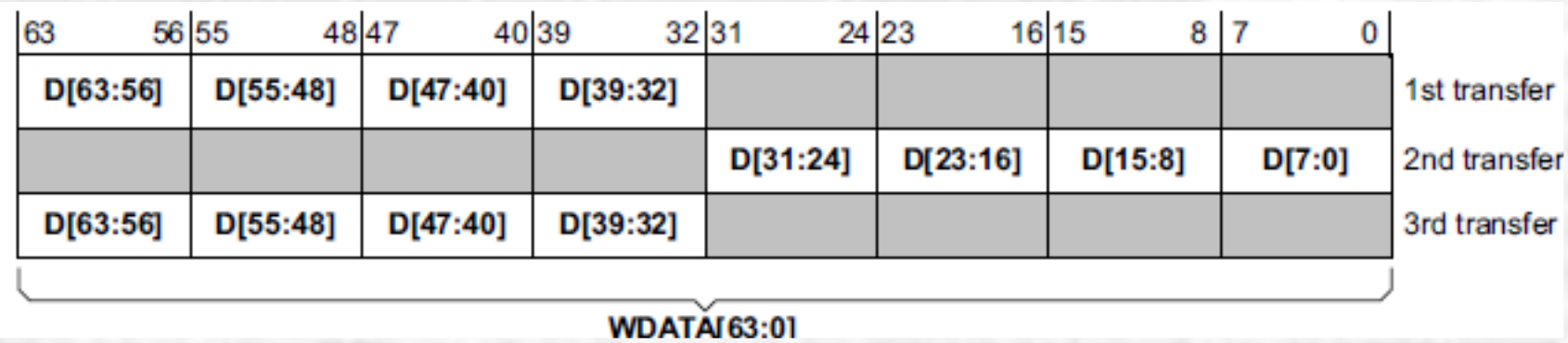
Byte lane shifts each transfer



Parallel Communications

On-chip Bus Structures

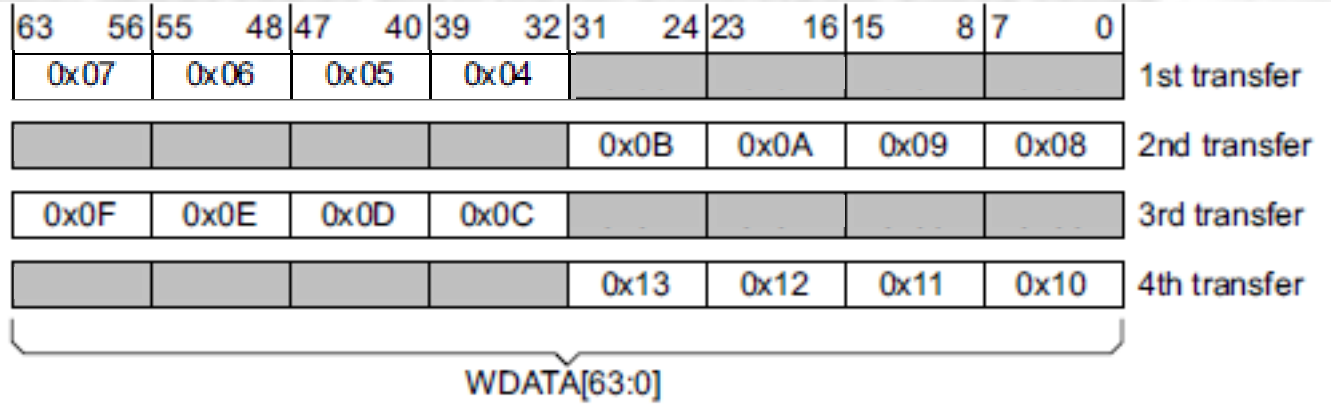
- AMBA – AXI Signaling - Data
  - Relationship between Data width and Beat Size
    - 4 Byte Beat
    - 3 Beat Burst
    - 64 bit data bus
    - 1st address = 0x04
    - Byte lanes shift each transfer



Parallel Communications

On-chip Bus Structures

- AMBA – AXI Signaling - Data
  - Relationship between Data width and Beat Size
    - 4 Byte Beat
    - 4 Beat Burst
    - INCR mode
    - 64 bit data bus
    - 1st address = 0x04

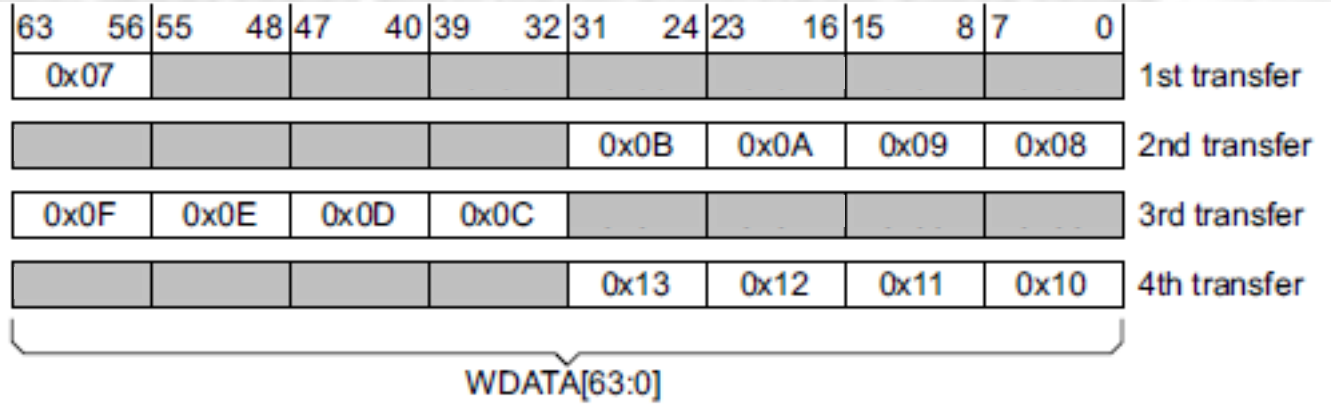


Parallel Communications

On-chip Bus Structures

- AMBA – AXI Signaling - Data
  - Relationship between Data width and Beat Size
    - 4 Byte Beat
    - 4 Beat Burst
    - INCR mode
    - 64 bit data bus
    - 1st address = 0x07

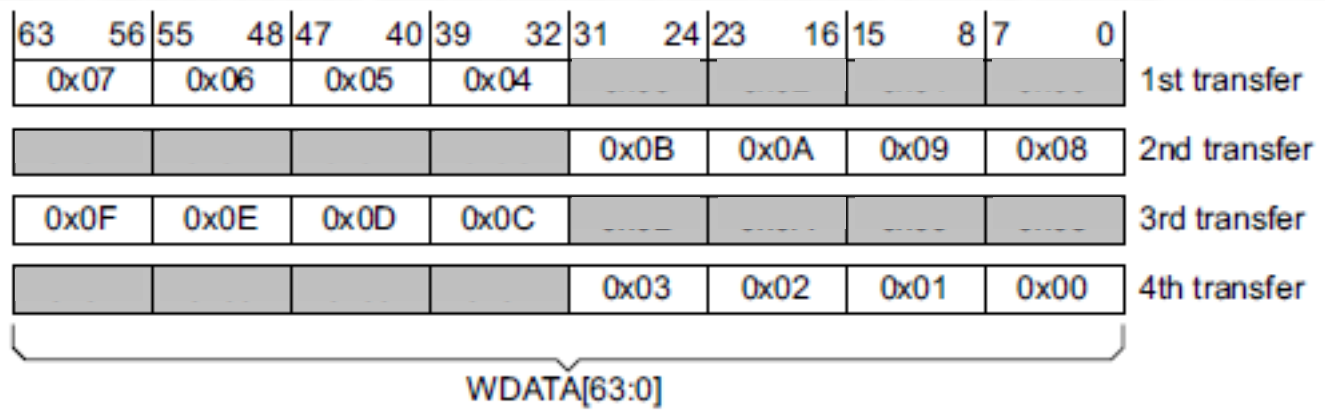
Un-aligned transfer



Parallel Communications

On-chip Bus Structures

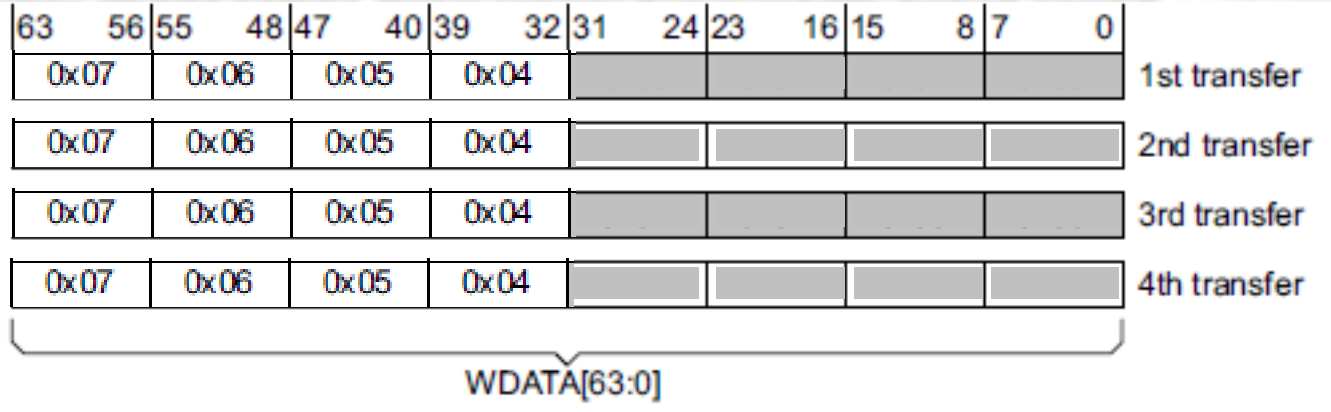
- AMBA – AXI Signaling - Data
  - Relationship between Data width and Beat Size
    - 4 Byte Beat
    - 4 Beat Burst
    - WRAP mode
    - 64 bit data bus
    - 1st address = 0x04



Parallel Communications

On-chip Bus Structures

- AMBA – AXI Signaling - Data
  - Relationship between Data width and Beat Size
    - 4 Byte Beat
    - 4 Beat Burst
    - Fixed mode
    - 64 bit data bus
    - 1st address = 0x04



Parallel Communications

On-chip Bus Structures

- AMBA – AXI Signaling - Data
  - Write Strobe
    - Indicates which data lane contains valid data
    - One strobe for each lane
    - WSTRB[n], where n is the number of bytes in the data bus

Parallel Communications

On-chip Bus Structures

- AMBA – AXI Signaling - Response
  - Read and Write transactions include a response
  - Read responses are part of the Read Data Channel – RRESP[1:0]
  - Write responses are on a separate Write Response Channel – BRESP[1:0]
  - Four responses
    - OKAY
    - EXOKAY
    - SLVERR
    - DECERR

RRESP[1:0] BRESP[1:0]	Response
0b00	OKAY
0b01	EXOKAY
0b10	SLVERR
0b11	DECERR

Parallel Communications

On-chip Bus Structures

- AMBA – AXI Signaling - Response
  - OKAY
    - Success of a normal access
    - Failure of an exclusive access
    - Exclusive access to a slave that does not support exclusive access
  - EXOKAY
    - Success of an exclusive access
  - SLVERR
    - Unsuccessful transaction – indicated by slave
      - FIFO over/under run
      - Write to Read only location
      - …
  - DECERR
    - Access to a non existent location
      - Typically handled by a dummy slave

Parallel Communications

On-chip Bus Structures

- AMBA – AXI Signaling – Transaction Identifiers
  - There is no strict relationship between the 5 channels in AXI
    - A read does not need to wait for data before doing something else
    - A write can do something else while waiting for the slave to respond with a READY signal
    - Write data must remain in order with respect to write addresses
  - This allows for multiple ongoing transactions – but how do you keep them straight?
    - Transaction identifier
    - Typically support 4-8 bits of identifier
      - 16 – 256 ongoing transactions

Transaction channel	Transaction ID
Write address channel	AWID
Write data channel, AXI3 only	WID[a]
Write response channel	BID
Read address channel	ARID
Read data channel	RID

Parallel Communications

On-chip Bus Structures

- AMBA – AXI Signaling – Transaction Identifiers
  - Rules
    - Transactions from different Masters have no order restriction
    - Transactions R/W with the same ID must remain in order
    - Transactions R – W – Resp with the same ID have no restrictions
    - Transactions with different IDs have no restrictions
    - Read and response transactions have no restrictions
    - Write Data must follow Write addresses
    - Transactions from 1 Master to multiple slaves with the same transaction ID must remain in order

Parallel Communications

On-chip Bus Structures

- AMBA AXI Signals

Global

Signal	Source
ACLK	Clock source
ARESETn	Reset source

Response

Signal	Source
BID	Slave
BRESP	Slave
BUSER	Slave
BVALID	Slave
BREADY	Master

Read Address

Signal	Source
ARID	Master
ARADDR	Master
ARLEN	Master
ARSIZE	Master
ARBURST	Master
ARLOCK	Master
ARCACHE	Master
ARPROT	Master
ARQOS	Master
ARREGION	Master
ARUSER	Master
ARVALID	Master
ARREADY	Slave

Read Data

Signal	Source
RID	Slave
RDATA	Slave
RRESP	Slave
RLAST	Slave
RUSER	Slave
RVALID	Slave
RREADY	Master

Write Address

Signal	Source
AWID	Master
AWADDR	Master
AWLEN	Master
AWSIZE	Master
AWBURST	Master
AWLOCK	Master
AWCACHE	Master
AWPROT	Master
AWQOS	Master
AWREGION	Master
AWUSER	Master
AWVALID	Master
AWREADY	Slave

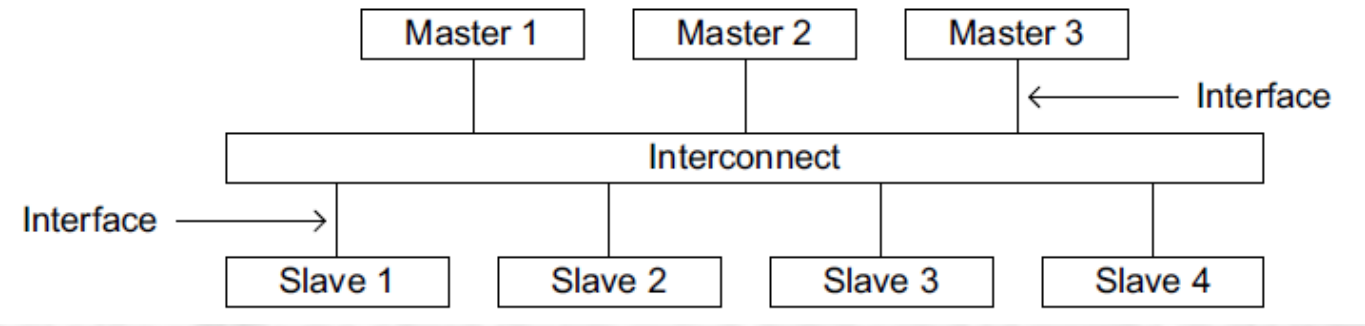
Write Data

Signal	Source
WID	Master
WDATA	Master
WSTRB	Master
WLAST	Master
WUSER	Master
WVALID	Master
WREADY	Slave

Parallel Communications

On-chip Bus Structures

- AMBA – AXI Interconnect
  - The interconnect ties Master to Slaves
    - 1::1
    - 1:: Many
    - Many :: 1
    - Many :: Many
  - Addresses used to identify source/destination
  - Transaction IDs appended with additional decode bits to differentiate Masters used to allow out of order operation



Parallel Communications

On-chip Bus Structures

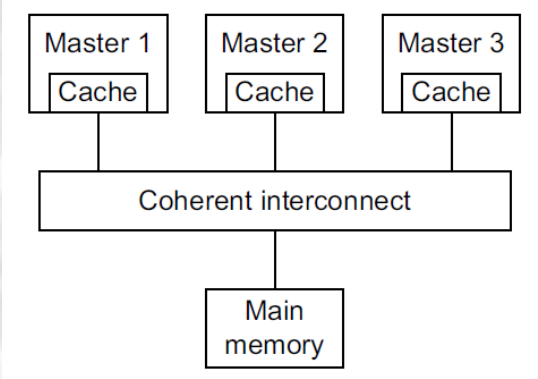
- AMBA – AXI Lite
  - All Burst Lengths are 1
  - All Data is full width 32b or 64b
  - All accesses are non-modifiable, non-bufferable, non-exclusive

Global	Write address channel	Write data channel	Write response channel	Read address channel	Read data channel
ACLK	AWVALID	WVALID	BVALID	ARVALID	RVALID
ARESETn	AWREADY	WREADY	BREADY	ARREADY	RREADY
–	AWADDR	WDATA	BRESP	ARADDR	RDATA
–	AWPROT	WSTRB	–	ARPROT	RRESP

Parallel Communications

On-chip Bus Structures

- AMBA – ACE
  - AXE Coherency Extensions
    - All Masters must see the same data
    - On a write to a location – all copies must be updated
    - Adds 3 channels + other signals + states
      - Snoop Address
      - Snoop Data
      - Snoop Response
    - Caches must support coherency extensions



Parallel Communications

On-chip Bus Structures

- AMBA – ACE
  - Cache Line states
    - Valid or in-valid
      - Data at this location is valid or not
    - Dirty or Clean
      - The data at this location has been modified since it was read in
    - Unique or shared
      - The data at this location is sharable or not

Parallel Communications

On-chip Bus Structures

- AMBA – ACE
  - Read
    - Master issues a read to it's cache at sharable address
    - Not in the local cache
    - Interconnect passes the request to other caches via the Snoop Address Channel
    - If any cache has the data (valid), it responds via the Snoop Response/Data Channel
    - Interconnect then provides the data to the Master (to be placed in cache locally)
    - If no copies are found Interconnect initiates a request to the next level of memory

Parallel Communications

On-chip Bus Structures

- AMBA – ACE
  - Write
    - Master issues a write to it's cache at sharable address
    - Interconnect passes the request to other caches via the Snoop Address Channel
    - If any cache has the data (valid), it clears the line in cache and it responds via the Snoop Response Channel that the data has been removed (invalidated)
    - If one of the valid lines was dirty, a write back is initiated before clearing
    - If a write back is required, Interconnect performs the writeback prior to writing to the local cache