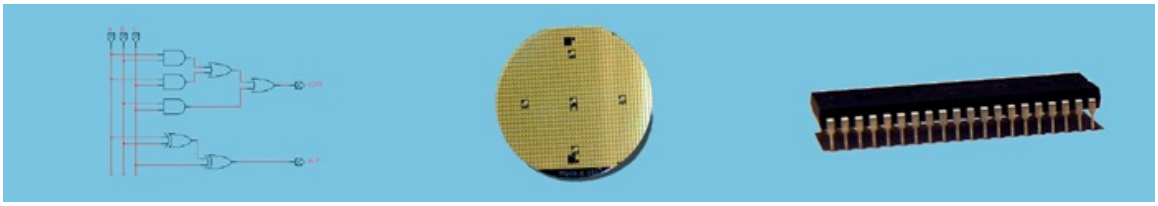
CE1900 WEEK 4 LABORATORY EXERCISES



LABORATORY SUMMARY

These laboratory exercises focus on the design and implementation of logic equations using both paper techniques and the VHDL hardware description language. Both **design methodologies** are important foundational skills for computer engineers.

Students will complete three design tasks:

- **Derive** canonical and K-map minimized Boolean logic equations.
- **Write** VHDL descriptions using Boolean logic statements.
- **Simulate** VHDL descriptions to verify circuit operation.

The laboratory exercises reinforce these CE1900 learning objectives:

- **Use** VHDL entry to design and simulate logic circuits.

Print this document and **bring** it to lab with the preliminary activities completed in the spaces provided. **Hint:** save your color print cartridge by selecting "black-and-white" printing from your print options.

REMEMBER

Complete all homework and preliminary lab exercises ***before you come to lab***.
Review the in-class laboratory exercises to preview the work you will do in the lab.

PRACTICE PROBLEMS

Test your progress in meeting your course learning objectives by completing these practice problems. Practice problems are for your personal study and may be collected and checked as part of your overall lab grade. **Ask** your instructor for help if needed.

1. **Design** and **implement** F(ABCD) = ∑m(2,3,6,11,12,14,15) using only a VHDL Boolean logic equation dataflow architecture for the ***K-map minimized*** equation. This type of architecture uses **and, or,** and **not** keywords instead of **with-select** or **when-else** keywords. **Use** Quartus to simulate your VHDL entity to verify correct operation.
2. **Design** and **implement** the K-map minimized function of problem one as a gate-level blueprint in Quartus. **Simulate** your blueprint to verify correct operation.
3. **Compare** and **contrast** the design approach taken in problems 1 and 2. **Compare** means to state how they are similar. **Contrast** means to state how they are different.
4. **Rewrite** the first exercise as a **with-select** dataflow architecture.

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PRELIMINARY LAB EXERCISES

Each student must complete these exercises before coming to the laboratory period.

1. **Design** and **simulate** a 4-bit numerical palindrome identifier. The palindrome identifier should produce 1 if and only if writing 4-bit number ABCD left-to-right is exactly the same as writing 4-bit number ABCD right-to-left. For example, 0110 is a 4-bit palindrome.

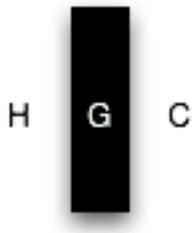
    a. **Complete** a paper or Microsoft Excel truth table for F(ABCD).
    b. **Write** the canonical equation.
    c. **Minimize** the canonical equation using a K-map. If no minimization is possible then the solution is the canonical equation.
    d. **Write** a VHDL description for the minimized equation.
    e. **Simulate** your VHDL circuit to verify correct operation by grouping the inputs into a bus and overwriting a binary count sequence from 0 to 15. **Set** the end time so that only one count sequence is shown.
    f. **Print** your VHDL description and simulation files.

2. **Design** and **simulate** a 4-bit packed-energy detector. The packed-energy detector produces a 1 if and only if all the energy in the four-bit number is side-by-side with no zeros between any energy bits. Examples of packed energy are ABCD = 1000, ABCD = 0001, and ABCD = 0110, ABCD = 0111, but 1001 is not packed-energy.

    a. **Complete** a paper or Microsoft Excel truth table for F(ABCD).
    b. **Write** the canonical equation.
    c. **Minimize** the canonical equation using a K-map. If no minimization is possible then the solution is the canonical equation.
    d. **Write** a VHDL description for your minimized equation.
    e. **Simulate** your VHDL circuit to verify correct operation by grouping the inputs into a bus and overwriting a binary count sequence from 0 to 15. **Set** the end time so that only one count sequence is shown.
    f. **Print** your VHDL description and simulation files.

3. **Design** and **simulate** a laboratory robot control circuit that ***follows*** the black line using only the left and right sensors, ***stops*** at speed bumps, ***and*** avoids collisions by ***backing up*** when a collision is sensed. All four motor control equations must be designed in this laboratory. Turns must be completed by ***turning off*** the appropriate motor.

a. **Start** by finishing a paper or Microsoft Excel truth table. **Include** don't care conditions when appropriate.



Normal Track with Centered Robot

Robot Over a Speed Bump

INPUTS				OUTPUTS				BEHAVIOR
D	**H**	**C**		**I**	**J**	**A**	**B**	
0	0	0						speed bump
0	0	1						
0	1	0						
0	1	1						
1	0	0						collision!
1	0	1						collision!
1	1	0						
1	1	1						

b. **Write** the canonical equations for I, J, A, and B.
c. **Minimize** the canonical equations with K-maps including don't cares.
d. **Write** the VHDL description for the minimized equations. **Note** that this is one project with a VHDL description containing all four equations.
e. **Simulate** your VHDL circuit to verify correct operation by grouping the inputs into a bus and overwriting a binary count sequence from 0 to 7. **Set** the end time so that only one count sequence is shown. **Print** your VHDL description and simulation files.

CE1900 WEEK 4 LABORATORY EXERCISES

The remainder of this document consists of laboratory exercises that must be completed during the laboratory period. **Read** through these exercises now to get a sense of the laboratory requirements. **Complete** the exercises during your assigned lab period.

LABORATORY EXERCISES

1. **Take** the weekly CE1900 quiz given by your instructor at the start of lab.
2. **Build** the robot in the laboratory and **debug** your circuit if necessary.
3. **Demonstrate** your working robot to the instructor.
4. **Demonstrate** your Quartus projects to the instructor. The instructor will complete the signature block at the end of this document. The signature block serves as proof that you have completed the laboratory assignments. **Keep** this document in your binder for CE1900 in case you need to refer to it in future work or in case the instructor asks to see the signature block again at a later date.
5. **Estimate** the total amount of time you spent working on the pre-lab and lab exercises. **Record** that time in minutes: _____

FOR INSTRUCTOR USE ONLY: DO NOT WRITE IN THIS TABLE

ITEM	COMMENTS	SCORE
Prelab		
VHDL and Quartus skills		

Instructor Signature: _____