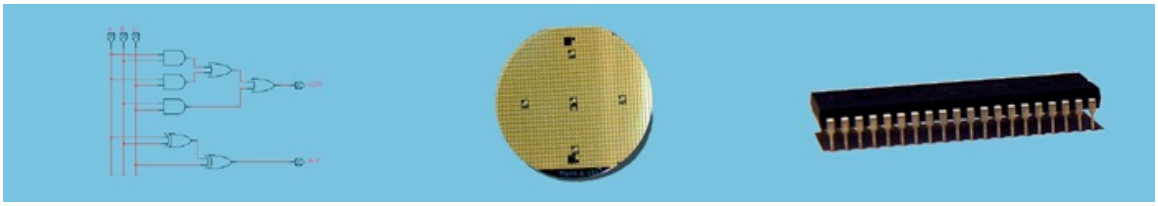
CE1900 WEEK 5 LABORATORY EXERCISES



LABORATORY SUMMARY

These laboratory exercises focus on the use of field-programmable gate arrays (FPGAs) as a platform to host digital designs. FPGAs contain a fabric of gates and multiplexer components that can be interconnected using internal fuses. Quartus creates a programming file for each project. Once design and simulation verify correct behavior, the programming file can be programmed into an Altera FPGA using a USB serial cable.

Students will complete three design tasks:

- **Write** a VHDL description using with-select assignment statements.
- **Simulate** the VHDL description to verify circuit operation.
- **Program** the project programming file into an Altera FPGA and verify operation.

The laboratory exercises reinforce these CE1900 learning objectives:

- **Use** VHDL entry to design and simulate logic circuits.
- **Implement** circuits in FPGAs.

Print this document and **bring** it to lab with the preliminary activities completed in the spaces provided. **Hint:** save your color print cartridge by selecting "black-and-white" printing from your print options.

REMEMBER

Complete all homework and preliminary lab exercises ***before you come to lab***.
Review the in-class laboratory exercises to preview the work you will do in the lab.

PRACTICE PROBLEMS

Test your progress in meeting your course learning objectives by completing these practice problems. Practice problems are for your personal study and may be collected and checked as part of your overall lab grade. **Ask** your instructor for help if needed.

1. **Design** and **simulate** F(ABCD) = ∑m(0,1,2,3,8,9) using a **K-map** and a **Quartus** schematic of your reduced equation. **Simulate** your circuit to verify correct operation.
2. **Design** and **simulate** F(ABCD) = 1 if and only if ABCD has an odd number of ones. In other words, 0000 would produce 0 but 0001, 0010, 0111, and others would produce 1. **Use** a Quartus VHDL with-select statement. **Simulate** your circuit to verify correct operation.

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PRELIMINARY LAB EXERCISES

Each student must complete these exercises before coming to the laboratory period.

1. **Design** and **simulate** a circuit that reports how many of four inputs bits have energy by turning on the appropriate number of output signals. In other words, given a number ABCD = 1010, the output WXYZ = 0011. Suppose each output signal drives a light-emitting diode (LED). Thus, ABCD has two inputs with energy and the output has two lights lit. Similarly, ABCD = 1110 produces an output of WXYZ = 0111 since three input signals have energy.

    a. **Complete** the truth table below.

INPUTS				OUTPUTS				BEHAVIOR
A	B	C	D	W	X	Y	Z	
0	0	0	0	0	0	0	0	all lights off, no input has energy
0	0	0	1	0	0	0	1	right most light on, one input has energy
0	0	1	0	0	0	0	1	right most light on, one input has energy
0	0	1	1					
0	1	0	0					
0	1	0	1					
0	1	1	0					
0	1	1	1					
1	0	0	0					
1	0	0	1					
1	0	1	0					
1	0	1	1					
1	1	0	0					
1	1	0	1	0	1	1	1	3 right most lights on, 3 inputs = 1
1	1	1	0	0	1	1	1	3 right most lights on, 3 inputs = 1
1	1	1	1					

b. **Create** a Quartus project and **use** a VHDL with-select description for the circuit. **Note** that this is one project with a VHDL description containing all four outputs equations as separate with-select statements.
c. **Simulate** your project to verify correct operation by grouping the inputs into a bus and overwriting a binary count sequence from 0 to 15. **Set** the end time so that only one count sequence is shown. **Print** your VHDL description and simulation files.

The remainder of this document consists of laboratory exercises that must be completed during the laboratory period. **Read** through these exercises now to get a sense of the laboratory requirements. **Complete** the exercises during your assigned lab period.

LABORATORY EXERCISES

1. **Take** the weekly CE1900 quiz given by your instructor at the start of lab.
2. **Check out** a DE1 FPGA board from EECS Tech Support.
3. **Scan** the manual for the DE1 FPGA board that you will find in the box. This manual is also available in PDF format on the CE1900 web page. **Identify** what you see in the manual on the DE1 board.

   A. **Look at** Figure 2.1 and identify the FPGA, the toggle switches that can be used as input signals, the RUN/PROG switch, as well as the red and green LEDs.
   B. **Look at** Chapter 4 briefly and pay particularly close attention to Table 4.1, Table 4.2, and Table 4.3.
   C. **Move** the RUN/PROG switch to the RUN position. **Never** use the DE1 with this switch in the PROG position during CE1900. In the RUN position, the programming file you program to the board will simply be used to run the board until power-off.
   D. **Note** the FPGA chip family (Cyclone II) and number (EP2C20F484C7) etched onto the top of the chip. These identification numbers are important in generating a correct programming file.
   E. **Scan** the information in Chapter 4 of the manual. This is the important chapter.
4. **Connect** the DE1 board to your computer using the USB cable. Windows should identify the device and try to install a driver. It will likely not install the driver for the USB blaster cable automatically. To install the driver, complete the following steps.

   A. **Go** to the Device Manager (search from Start Menu for those words).
   B. **Right-click** on USB-Blaster under "Other Devices"

C. **Click** "Update driver software…"
D. **Click** "Browse my computer for driver software"
E. **Browse** to C:\altera\13.0sp1\quartus\drivers. **Do not go** into a sub-directory in this folder. **Note** that if you installed Quartus on your D: driver then you should browse to D:\altera\13.0sp1\quartus\drivers.
F. **Click** Next
G. **Click** "Install" when the question "Would you like to install this device software…" appears.
H. **Click** Ok, Ok, Next.
I. **Receive** a success message that "Altera USB-Blaster" has been installed.
J. **Click** Close.

5. **Assign** the correct FPGA device in Quartus.

A. **Choose** Assignments:Device in Quartus.
B. **Choose** the Cyclone II family.
C. **Choose** the EP2C20F484C7 device from the Available Devices panel.
D. **Click** OK.

6. **Assign pins** for your inputs and outputs.

A. **Choose** Assignments:Pin Planner
B. **Use** the All Pins panel to **assign** A, B, C, D to pins that are connected to the toggle switches as shown in Table 4.1. For example, if you want A attached to toggle switch 0, you would type PIN_L22 in the location field for signal A. **Note** that if the All Pins panel is not visible, you can make it visible through the View menu.
C. **Use** the All Pins panel to **assign** W, X, Y, and Z to four of the green LEDs. **Refer** to Table 4.3.

7. **Build** the programming file by clicking the **compile** toolbar button.
8. **Program** the FPGA using the Tools:Programmer dialog box.

A. **Click** the Hardware Setup button.
B. **Double-click** the USB Blaster.
C. **Click** the Close button.
D. **Ensure** the Program/Configure checkbox is checked.
E. **Click** the Start button.

9. **Verify** that your circuit works by comparing its behavior against your truth table.
10. **Demonstrate** your laboratory work to the instructor.

11. **Return** your equipment to EECS Tech Support

A SPECIAL NOTE FOR COMPUTER ENGINEERING STUDENTS

Computer engineering students are required to purchase a DE0 FPGA board in CE1910 next quarter. The boards are available for purchase now if you would like to purchase early. They may be purchased from EECS Tech Support for $80. The cost is charged to your student account. The steps for device assignment, pin assignment, and programming are identical except that the device family is Cyclone III and the chip number is EP3C16F484C6(N). Note that the DE0 manual is also located on the CE1900 laboratory web page and it shows appropriate pin numbers for switches, LEDs, etc. in its tables.

Software engineering students are not allowed to purchase the DE0 board from EECS Tech Support as they do not take CE1910 and thus the quantity ordered is insufficient to allow purchase. Software engineering students should use DE1 boards checked out from EECS Tech Support.

FOR INSTRUCTOR USE ONLY: DO NOT WRITE IN THIS TABLE

ITEM	COMMENTS	SCORE
Prelab		
VHDL and Quartus skills		

Instructor Signature: _____