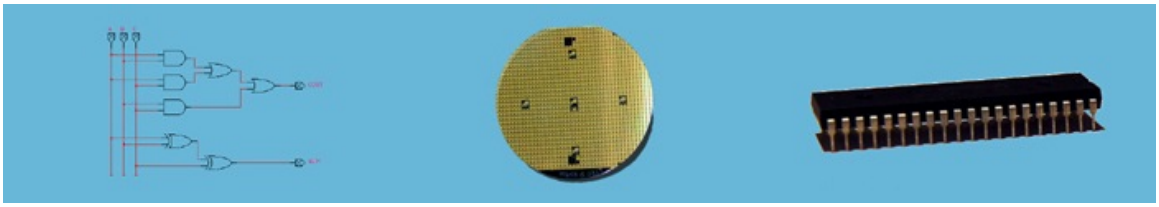
CE1900 WEEK 7 LABORATORY EXERCISES



LABORATORY SUMMARY

These laboratory exercises implement more of the basic computer arithmetic circuits studied in lecture by using the Quartus toolset to design, simulate, and program the circuits into programmable logic devices on the Altera DE1 laboratory board. The DE1 hosts one Altera Cyclone II field programmable gate array. The laboratory board is a fixed platform and the chips should not be removed. A set of switches and wire headers are included to allow input voltages to be connected. A set of light-emitting diodes (LEDs) and 7-segment displays are included to allow system results to be displayed to the user. This week, students practice VHDL description, schematic blueprints, simulation, and implementation.

Students will complete three design tasks:

- **Enter** a VHDL description for a full-adder component.
- **Enter** a VHDL description for a 7-segment display decoder.
- **Enter** a structural VHDL description of a 4-bit add-subtract circuit.
- **Enter** the top-level system schematic diagram.
- **Implement** the top-level system using the Cyclone II.
- **Test** the system in the laboratory.

The laboratory exercises reinforce these CE1900 learning objectives:

- **Use** VHDL description to design and simulate arithmetic circuits.
- **Implement** completed schematic designs in programmable logic devices.

Print this document and **bring** it to lab with the preliminary activities completed in the spaces provided.
Hint: save your color print cartridge by selecting "black-and-white" printing from your print options.

REMEMBER

Complete all homework and preliminary lab exercises ***before you come to lab***.
Review the in-class laboratory exercises to preview the work you will do in the lab.

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PRACTICE PROBLEMS

Take a break from practice exercises this week. Instead, focus on reading the on-line VHDL tutorials, working the extensive pre-laboratory exercises, and reviewing your lecture notes during your study times.

PRELIMINARY LAB EXERCISES

READ THESE DIRECTIONS CAREFULLY AS YOU COMPLETE THE PRELAB WORK.

1. **Create** a new Quartus project called **lab7**. This is the **only project** you will create during this lab.
2. **Write** a VHDL **logical** description for a full adder (FA).
3. **Write** a VHDL **with-select** description file for a seven-segment decoder (SEG7DECODE). This entity decodes a 4-bit twos complement signed binary number into left and right 7-segment displays. The left display displays a negative sign for negative numbers and is blank for positive numbers. The right display shows the magnitude of the number from. Thus, the display will read from -8 to 7.
4. **Write** a VHDL **structural** description for the 4-bit add-subtract circuit shown in Figure 1. **Use** your FA entity as a component, declare internal signals for the ripple carries, and use port maps to drop components into your diagram. One nice feature of the VHDL port map is the ability to use logic equations in the mapping. Thus, you can do B(0) xor SUB right inside the port map statement. **DO NOT DRAW SCHEMATICS. THIS IS VHDL ONLY!**

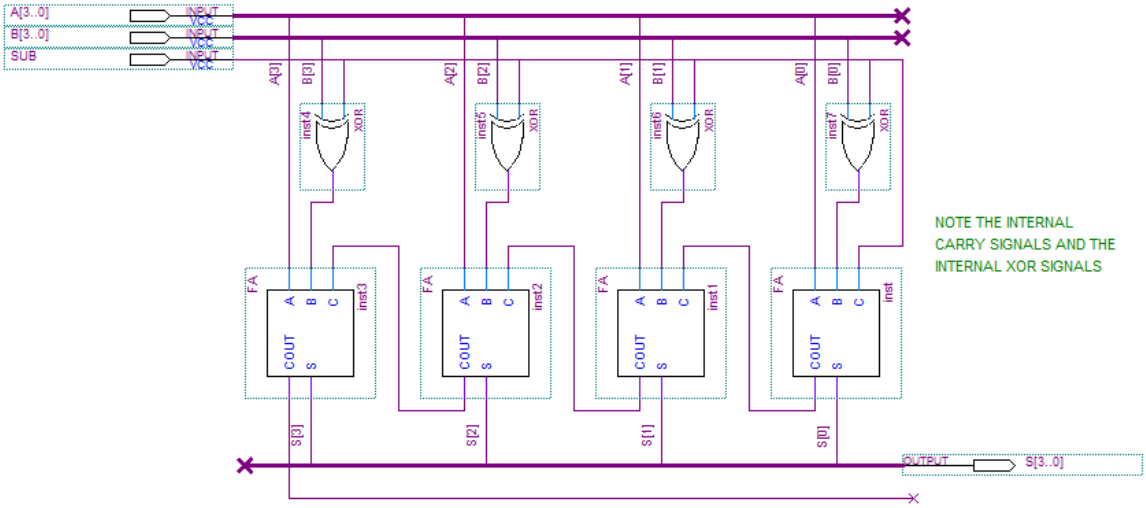

Figure 1: A 4-bit add-subtract circuit

5. **Write** a VHDL **structural** description for the top-level entity called **lab7**. **Use** Figure 2 as a guide.

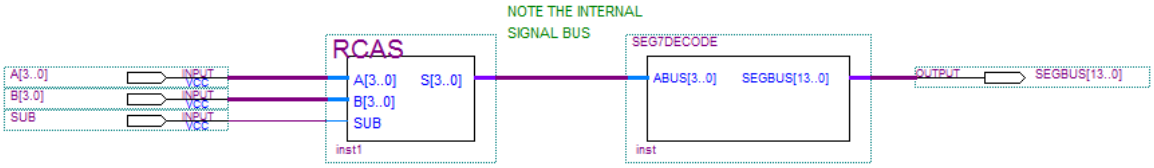

Figure 2: The lab7 project schematic

6. **Correct** any VHDL errors discovered during analysis and elaboration of the project.
7. **Simulate** your circuit.
8. **Make** device and pin assignments for laboratory testing. **Use** the Cyclone II, the 7-segment displays, and the toggle switches available on the DE1 board. **Use** switches 7 down to 4 as A[3], A[2], A[1] and A[0]. **Use** switches 3 down to 0 as B[3], B[2], B[1], and B[0]. **Note** that the DE1 manual is available as a PDF on the lab page of the course website. **Computer Engineering** students that have purchased the DE0 board early can use the DE0 with appropriate chip and pin assignments.

LABORATORY EXERCISES

Each student must complete these exercises on their own time during week 7. **Your instructor will tell you if you have to come to the lab period to take a quiz, if you will have an online quiz, or if you will not have a quiz this week.**

1. **Check** out a DE1 board from EECS Tech Support.
2. **Assign device and pins, compile** the design and **program** it into the CYCLONE II FPGA.
3. **Test** your design.
4. **Capture** a cell phone photo of your working circuit for a several different inputs A and B. **Choose** inputs that give both positive and negative numbers.
5. **Write** a short laboratory report document in Microsoft Word. **Include** your VHDL code, simulation diagrams, and the circuit diagrams designed by Quartus. You can find these diagrams through Tools:Netlist Viewers:RTL View. **Remember** to double-click on components like RCAS to see the internal circuit. **Submit** this report according to the instructions given to you by your professor.