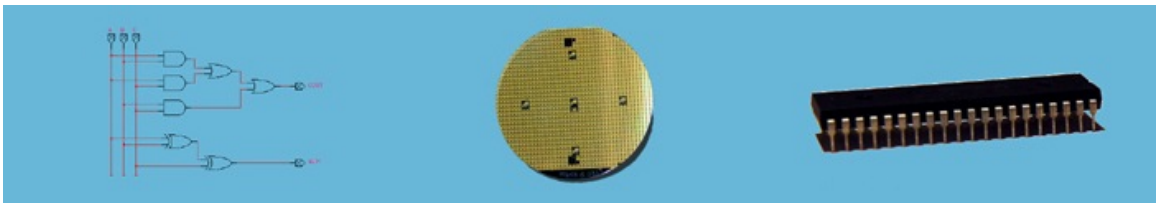
CE1900 WEEK 8 AND 9 LABORATORY EXERCISES



LABORATORY SUMMARY

Students have learned a significant amount about digital logic design. Take a look at the knowledge base developed so far:

- Signal theory: analog and digital signals, voltage levels, power, and ground
- Number systems: binary, octal, hexadecimal, basic Boolean algebra laws
- Standard logic gates: not, and, or, nand, nor, xor, xnor, 7400 family chips
- Standard components: full adder, ripple carry adder, ripple carry adder-subtractor, ALU
- Paper design techniques: truth tables, canonical equations, K-map reduction, timing diagrams
- Computer aided design: VHDL descriptions, schematic blueprints, simulation, FPGA platforms

This **laboratory exercise** reinforces the knowledge of ALU design. Students will complete multiple design tasks and follow this schedule of deliverables.

- Week 8: In-lab work on ALU design. **Students must attend their laboratory period**.
- **Due Week 9:** Laboratory demonstration of the working ALU on the laboratory DE1 board.

The laboratory exercises reinforce these CE1900 learning objectives:

- **Use** VHDL entry to design and simulate arithmetic circuits.
- **Implement** completed designs in programmable logic devices.

Print this document and **bring** it to lab with the preliminary activities completed in the spaces provided.
Hint: save your color print cartridge by selecting "black-and-white" printing from your print options.

REMEMBER

Complete all homework and preliminary lab exercises ***before you come to lab***.
Review the in-class laboratory exercises to preview the work you will do in the lab.

PRACTICE PROBLEMS

Test your progress in meeting your course learning objectives by completing these practice problems. Practice problems are for your personal study and will not be graded. **Ask** your instructor for help understanding the problems if needed.

1. **Complete** this abstract truth table for a 4-bit ALU with 8 functions. The table is "abstract" because the outputs are stated as A, B, A and B, A or B, etc. rather than binary numbers. Think about what the extenders need to pass to the full adder inputs.

S	ALU OUTPUT F	LE OUTPUT X	AE OUTPUT Y	CE OUTPUT C0
0	constant 0			
1	constant 1			
2	constant -1			
3	B	B	0	0
4	-B			
5	A+B	A	B	0
6	A-B			
7	A NOR B			

2. **Implement** the logic extender from problem 1 as a VHDL entity using a with-select dataflow architecture. **Simulate** your design in Quartus to verify correct operation.
3. **Use** a K-map to derive the arithmetic extender equation from problem 1.
4. **Describe** why the carry extender is ***only used*** for the least significant column of the ALU.
5. **Practice** your twos-complement binary numbers by finding the 8-bit twos complement encoding for the numbers: -100, +28, -36, -72, -1, +49, +117, -55, -25, +88.

PRELIMINARY LAB EXERCISES

Given these reference figures:

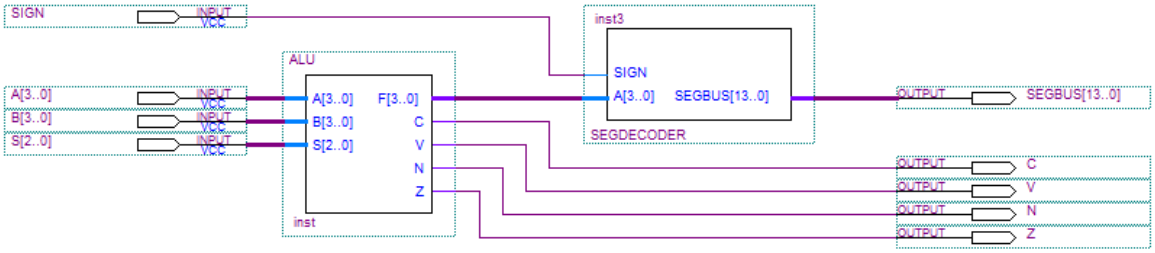


Figure 1: The final laboratory system

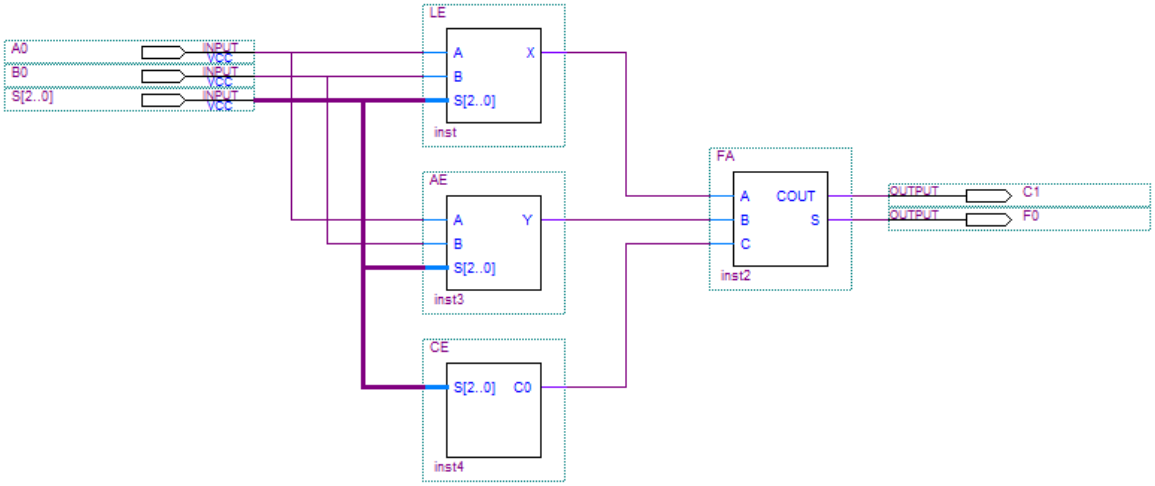


Figure 2: The ALU bit slice for column 0 of the calculation.

1. **Complete** the truth-table design for this ALU bitslice:

INPUTS			OPERATION	OUTPUTS		
s2	**s1**	**s0**		**X**	**Y**	**C0**
0	0	0	A and B			
0	0	1	A or B			
0	1	0	A xor B			
0	1	1	B + B (mult2)			
1	0	0	B – 1 (dec)			
1	0	1	A + 1 (inc)			
1	1	0	A – B (sub)			
1	1	1	A + B (add)			

2. **Create** a new folder on your computer to hold the ALU design project.
3. **Complete** these design files.

   A. VHDL descriptions of the FA, AE, LE, and CE components of the ALU.
   B. VHDL description of the display decoder that displays the numeric result in either signed or unsigned format based on the binary value of the SIGN input. Display 0 through 15 for unsigned calculations and -8 through 7 for signed calculations.
   C. VHDL structural description of the 4-bit ALU. Note that the output bits C, V, N, and Z may not have been discussed in lecture. The C bit is the carry out and represents unsigned overflow. The V bit is signed overflow and can be found using an exclusive-or of the two most significant carry bits. The N bit is true whenever the most significant F bit is true. The Z bit is true when F = 0.
   D. VHDL structural description of the ALU with decoder. This is the final design.

4. **Complete simulation** by overwriting a constant value onto A and B and overwriting a count sequence onto the selection signal S. This will allow you to verify that all 8 functions operate correctly. **Choose** a random value for A and a random value for B.

5. **Print** well-commented VHDL files and the simulation results. **Submit** these VHDL deliverables to the instructor at the timer of your demonstration. **VHDL will be graded based on quality and the included comments that document your work.**

LABORATORY EXERCISES

Each student must demonstrate the ALU by the end of the week 9 laboratory period. .

1. **Take** the weekly CE1900 quiz given by your instructor at the start of the laboratory.
2. **Implement** the lab design in the DE1 laboratory board during the week 9 lab period. **Use** three pushbutton switches for the ALU selection bits, toggle switches for A and B, a toggle switch for the sign control signal of the display decoder, two 7-segment displays, and red LEDs for the ALU C, V, N, and Z bits. **Computer engineers** that purchased the DE0 board early can use appropriate chip and pin assignments for that board.
3. **Test** the DE1 implementation to **verify** operation.
4. **Demonstrate** to the instructor. The instructor will complete the signature block at the end of this document. The signature block serves as proof that you have completed the laboratory assignments. **Keep** this document in your binder for CE1900 in case you need to refer to it in future work or in case the instructor asks to see the signature block again at a later date.
5. **Estimate** the total amount of time you spent working on the pre-lab and lab

   exercises. **Record** that time in minutes: _____

6.

FOR INSTRUCTOR USE ONLY: DO NOT WRITE IN THIS TABLE

ITEM	COMPLETED	SCORE
Design exercises		
Demonstrates understanding of Quartus		
Lab demonstration		

Instructor Signature: _____