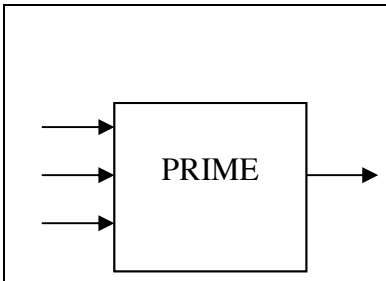
SCHEMATIC DESIGN IN QUARTUS

Consider the design of a three-bit prime number detector. The block diagram and truth table are shown in Figure 1. The inputs are signals named A, B, and C and the output is a signal named PRIME. Note that this example calls 1 a prime number for the purposes of illustrating equation simplification. The mathematical definition of a prime number would not consider 1 to be prime.



A	B	C	PRIME
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	0
1	1	1	1

Figure 1: A Prime Number Detector

Test your progress with the course learning objectives by deriving the canonical and minimized equations. Calculate the gate reduction ratio. Use the space on this page to complete your work.

Print out this tutorial and work your solution below or on the next page in weeks 2 or 3 of the quarter as part of your study time. Do not attempt to work this problem in week 1 of the quarter because lecture will not have covered enough material. Simply move on with the tutorial.

This document will illustrate how to create a Quartus schematic project to draw and simulate the prime number detector.

THIS PAGE INTENTIONALLY LEFT BLANK -- USE IT FOR PRACTICE LATER IN THE QUARTER

1. **Pin** Quartus to your Start menu so that it is easy to find each time you need it.
   A. **Right-click** on Start Menu : All Programs : Altera Web Edition : Quartus II Web Edition : Quartus II (64 bit) and **choose** Pin to Start Menu.
   B. **Note** that in the menu descriptions in item A above, the version number of Quartus, 13.0.1, for example was removed. This allows this document to be generic and usable across versions as Quartus updates software quite regularly.

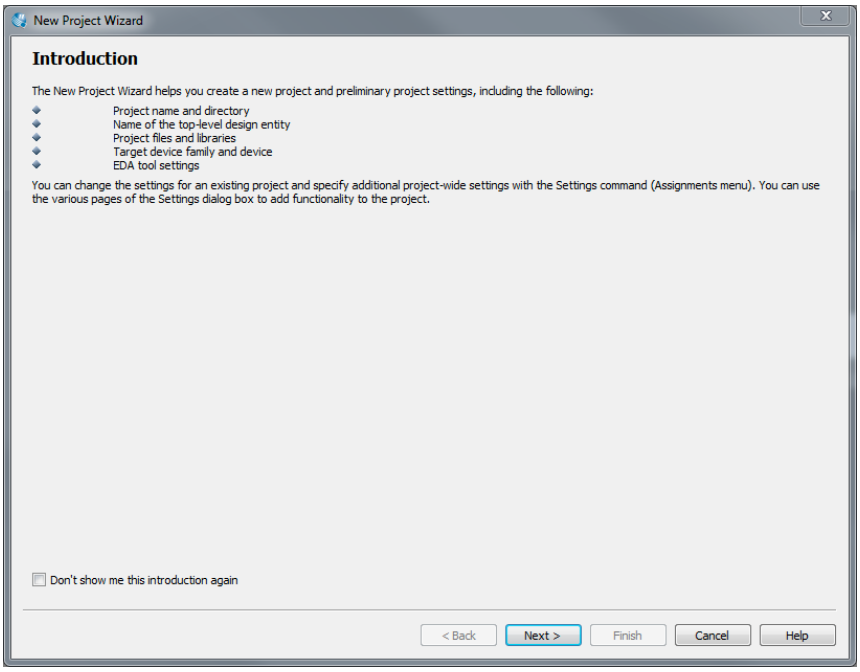
2. **Start** Quartus. It will present you with the standard blank startup window.

Quartus may present a Tools and Tips dialog box on first startup.
Simply close the window.

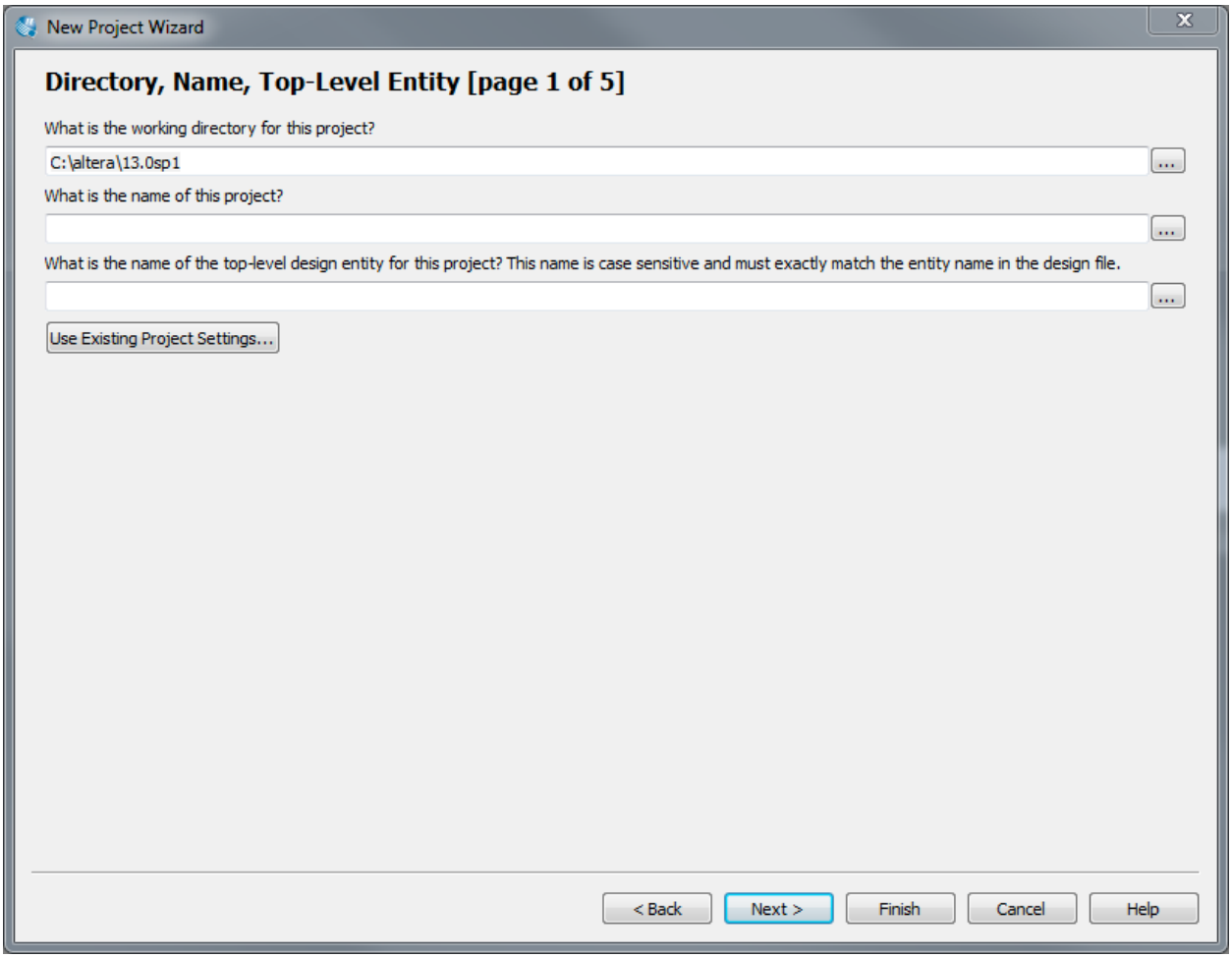
Quartus may present other dialog boxes on first startup.
Simply close them until you see something similar to the screenshot/].

3. **Create** a new project for your circuit design by **choosing** “New Project Wizard” from the “File” menu. A project is a collection of files completing the circuit design. Every functional block (black box) in the schematic will have at least one file associated with it.

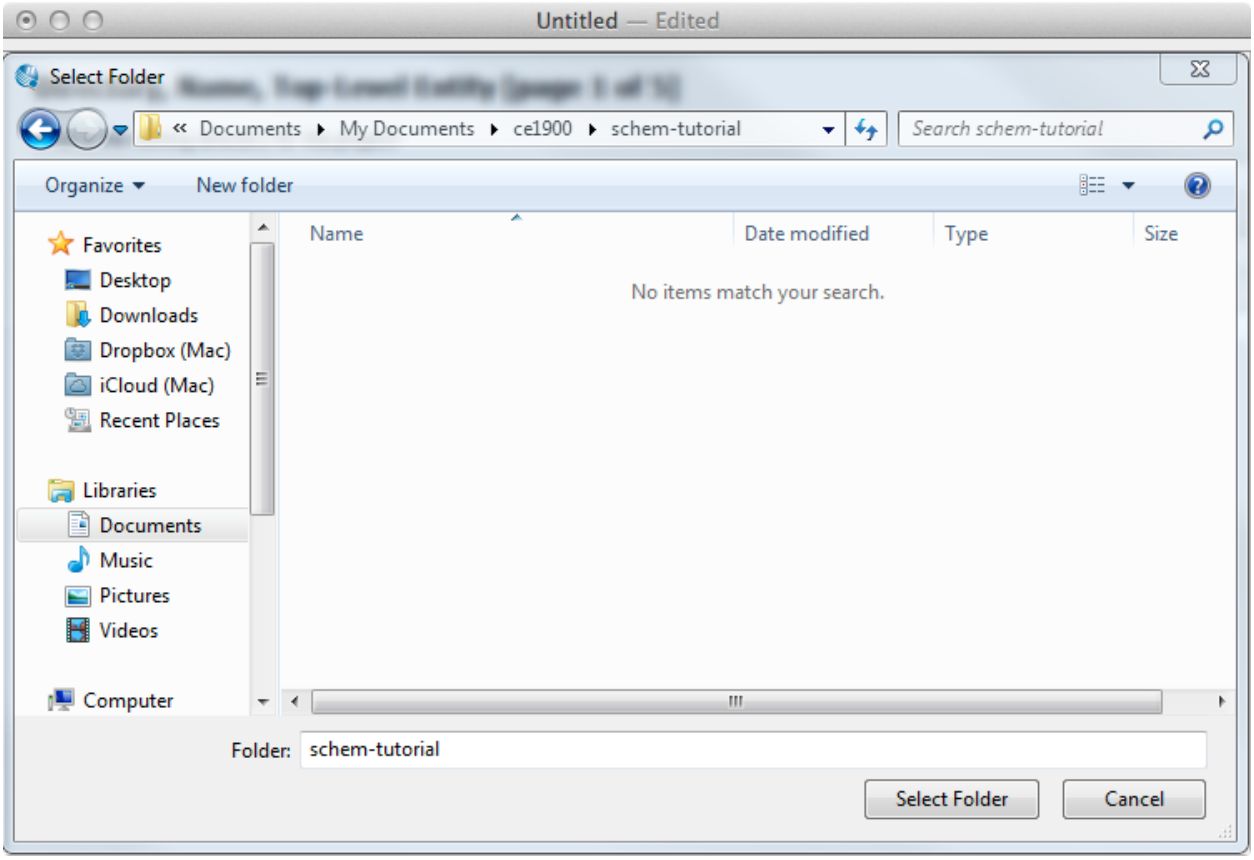
4. Click the “Next” button to advance beyond the information dialog box.



5. **Click** the "…" button next to the working directory textbox.

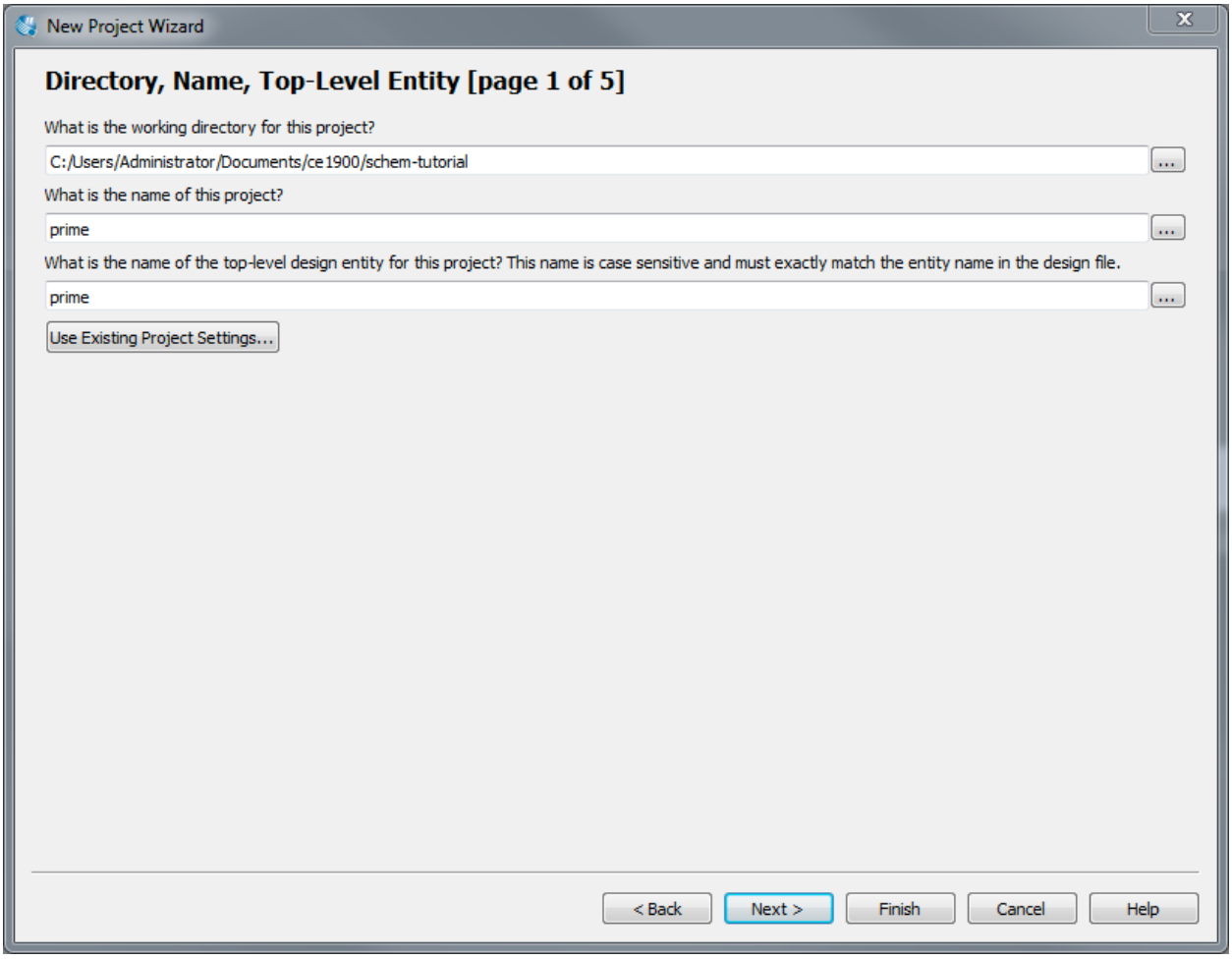


6. **Create** a project folder for your project work.
   A. **Browse** to your Documents folder using the side bar in the file browser.
   B. **Create** a CE1900 folder using the New Folder choice above the side bar.
   C. **Double-click** the CE1900 folder to move inside of it.
   D. **Create** a schematic tutorial folder. In this example, it's called schem-tutorial.
   E. **Double-click** the schem-tutorial folder to move inside of it.
   F. **Choose** Select Folder.

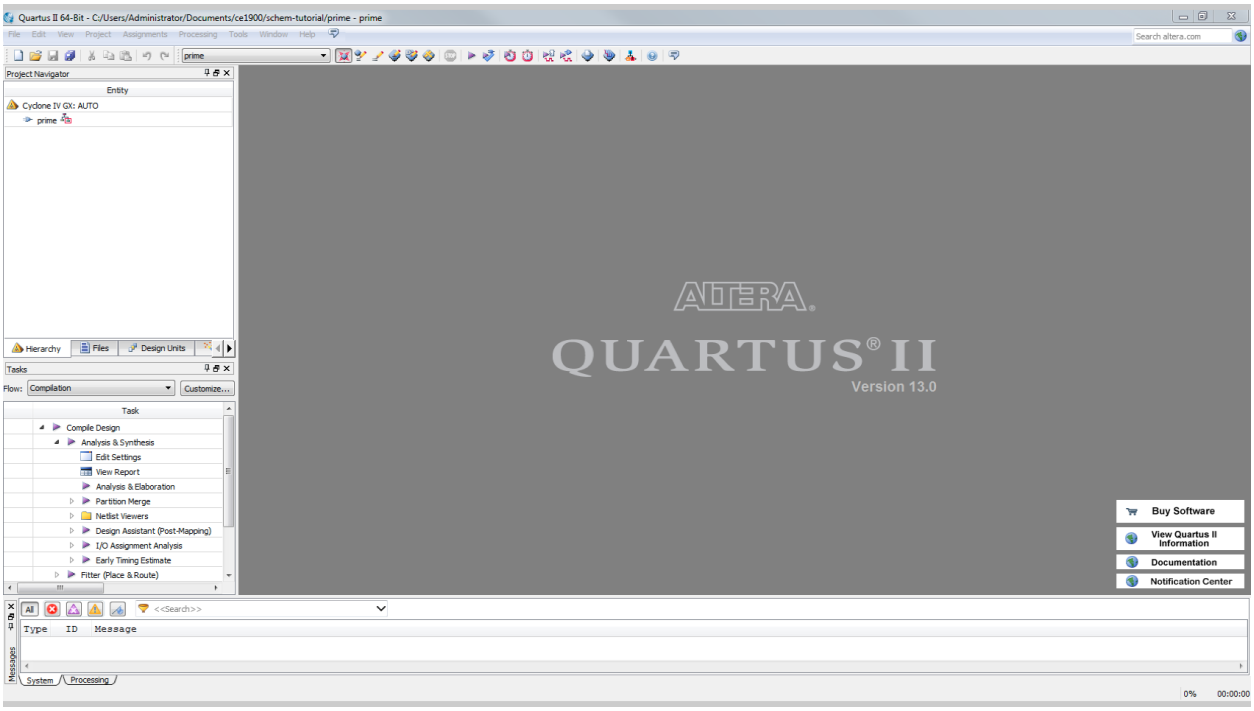


Look closely at the screenshot. The instructors recommend you make a CE1900 folder inside your My Documents folder. Projects folders are then placed inside this CE1900 folder.

7. **Name** the project and top-level entity “prime”. Simple projects with a single functional block – like this one – usually have the project and entity names matching. More complicated projects may have different names. Examples of this type of project will be seen later in the quarter. **Click** the “Finish” button.

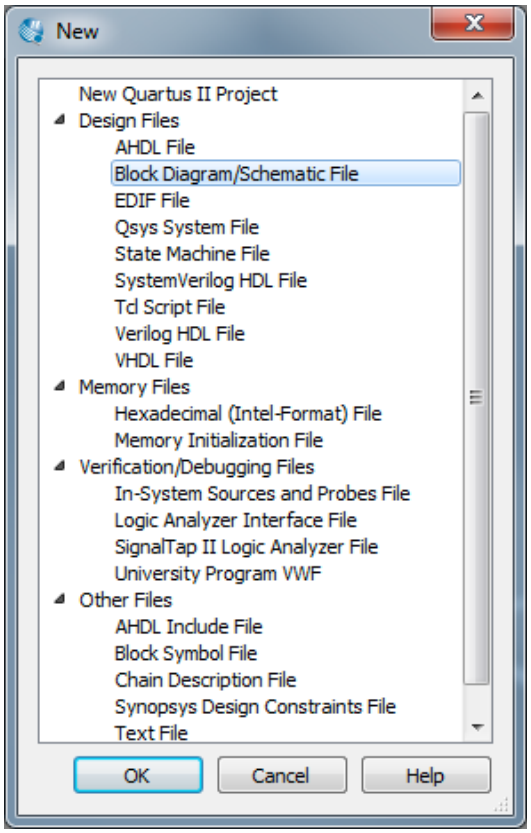


8. **Note** the entity file named “prime” in the project hierarchy tab on the left of the screen.



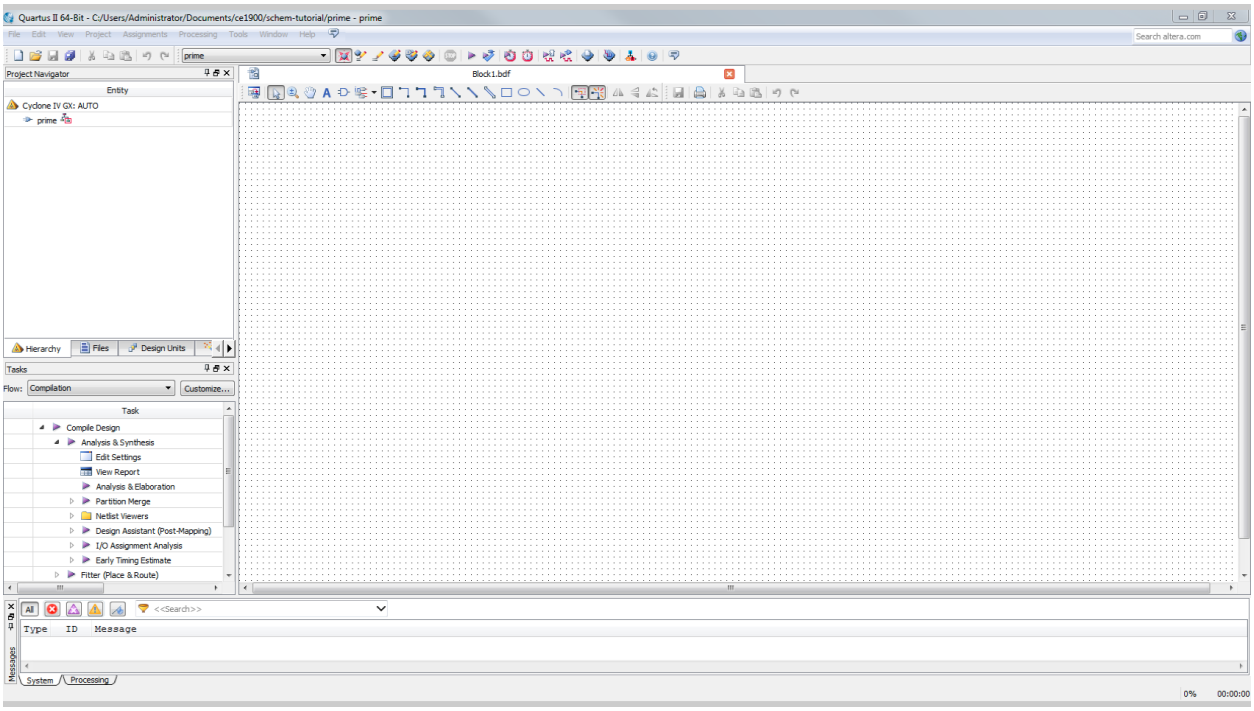
The Project Navigator can always be opened if you accidently close it by choosing View:Utility Windows:Project Navigator from the menus.

9. **Add** the schematic diagram for entity prime.
   A. **Choose** the “new” icon, the “New...” choice from the “File” menu, or by typing ctrl-n. The “New” dialog box will appear.
   B. **Highlight** “Schematic File”.
   C. **Click** the “OK” button.



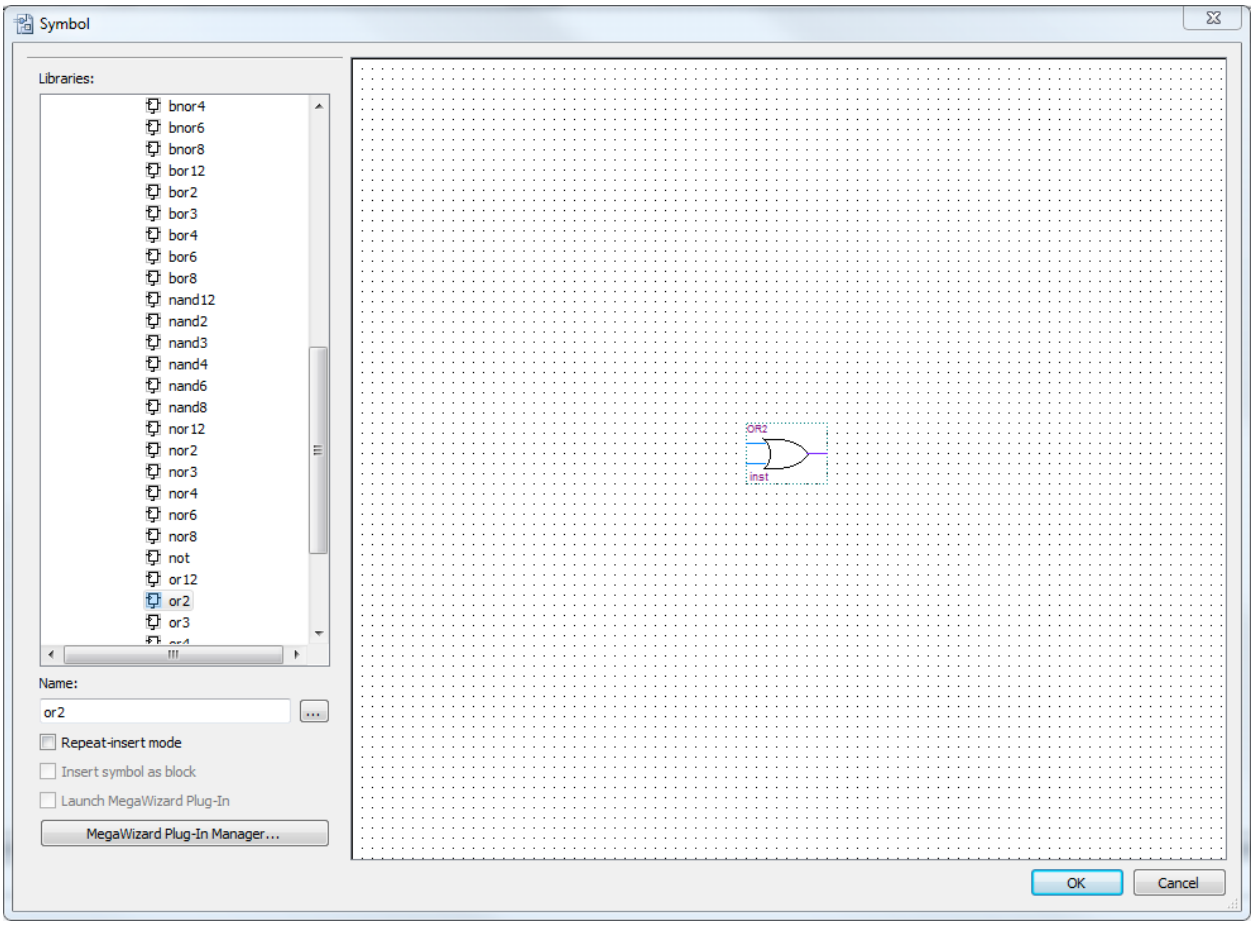
Schematic diagrams are blueprints of digital computer circuits.

10. **Click** the “Maximize” button to the left of the red “X” close button to bring the schematic size full-screen.



Quartus is a Windows application. You will feel quite comfortable with the menu structure, maximizing, minimizing, saving, and printing.

11. **Double-click** inside the schematic grid to call-up the component library symbol browser.
    A. **Note** that this example has expanded the library to see the basic logic gates.
    B. **Note** that you can also type the name of the component in the “Name” textbox to quickly locate it.
    C. **Select** the 2-input OR gate (OR2) to get started building the minimized equation for function PRIME. **Click** Ok.

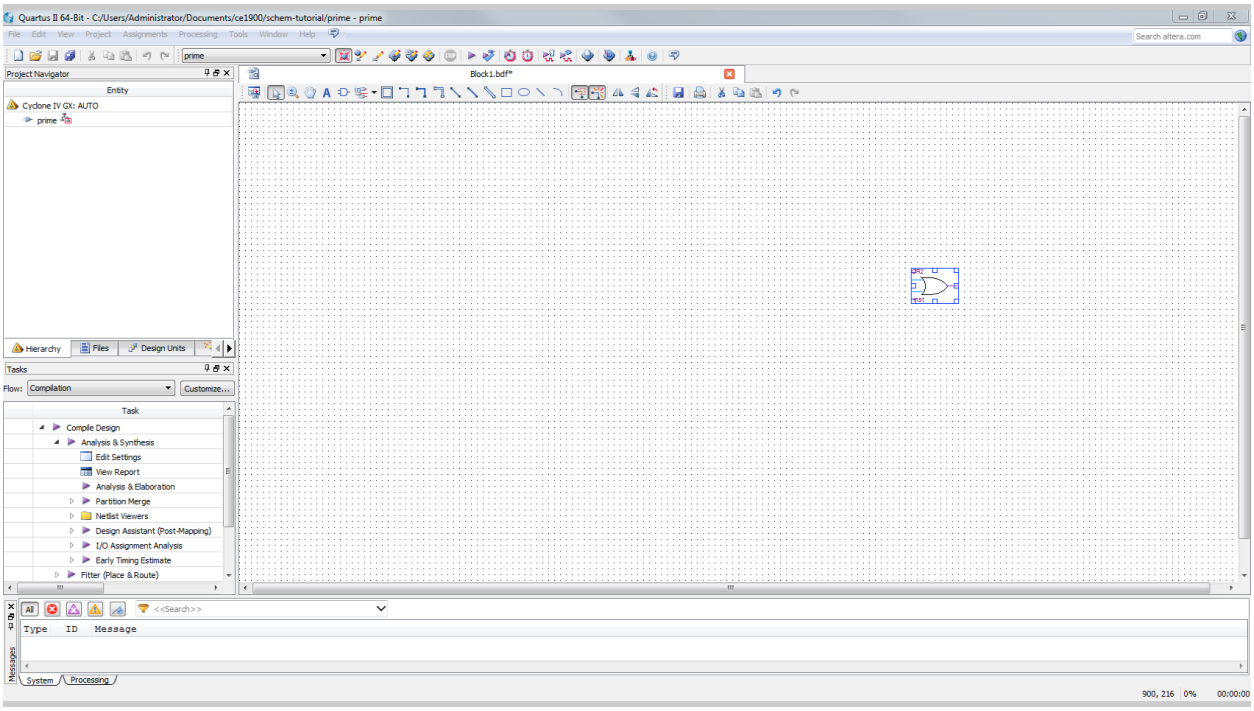


TEST YOUR PROGRESS RESULTS:

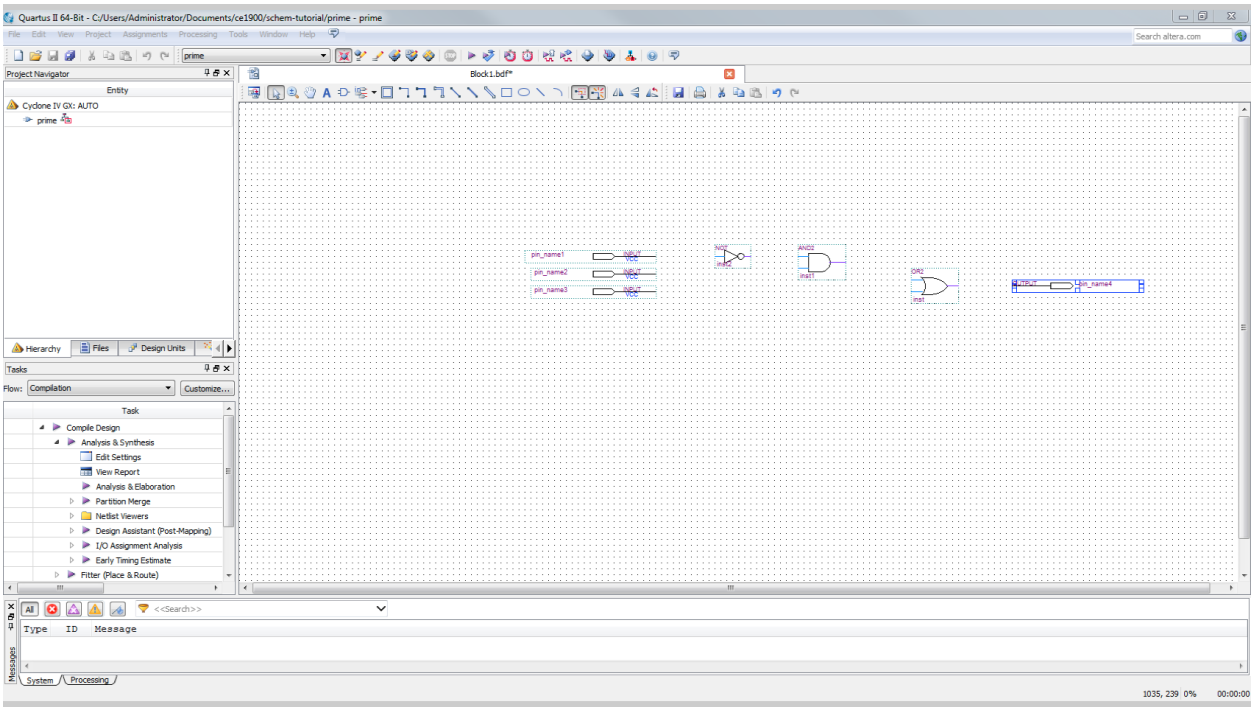
The canonical equation is: PRIME=!m(1,2,3,5,7)=A’B’C+A’BC’+A’BC+AB’C+ABC
The minimized equation is: PRIME=A’B+C

These are the answers you should get during your study time in weeks 2 or 3 of the quarter!

12. **Place** the OR2 component toward the right-hand side of the schematic by rolling the mouse into position and clicking the mouse button.

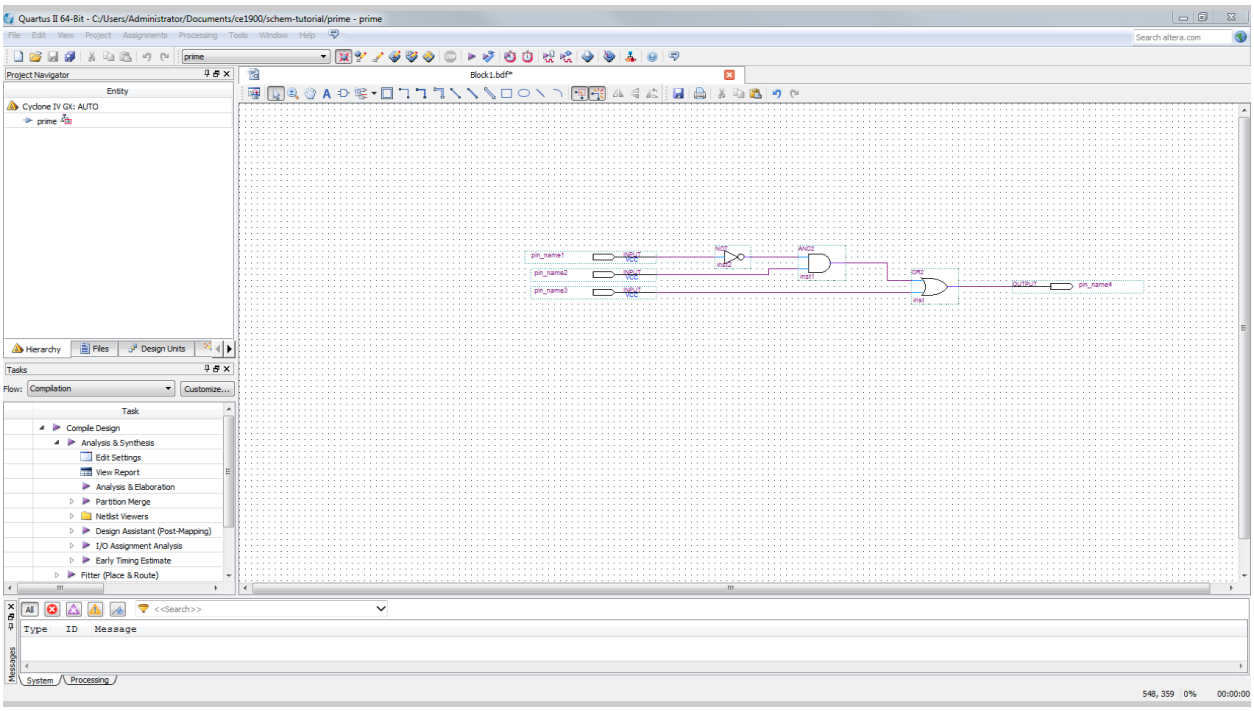


13. **Place** an AND2 component, a NOT component, three input components, and one output component.



Remember that you can get to the library by "double-clicking" in blank space on the schematic.

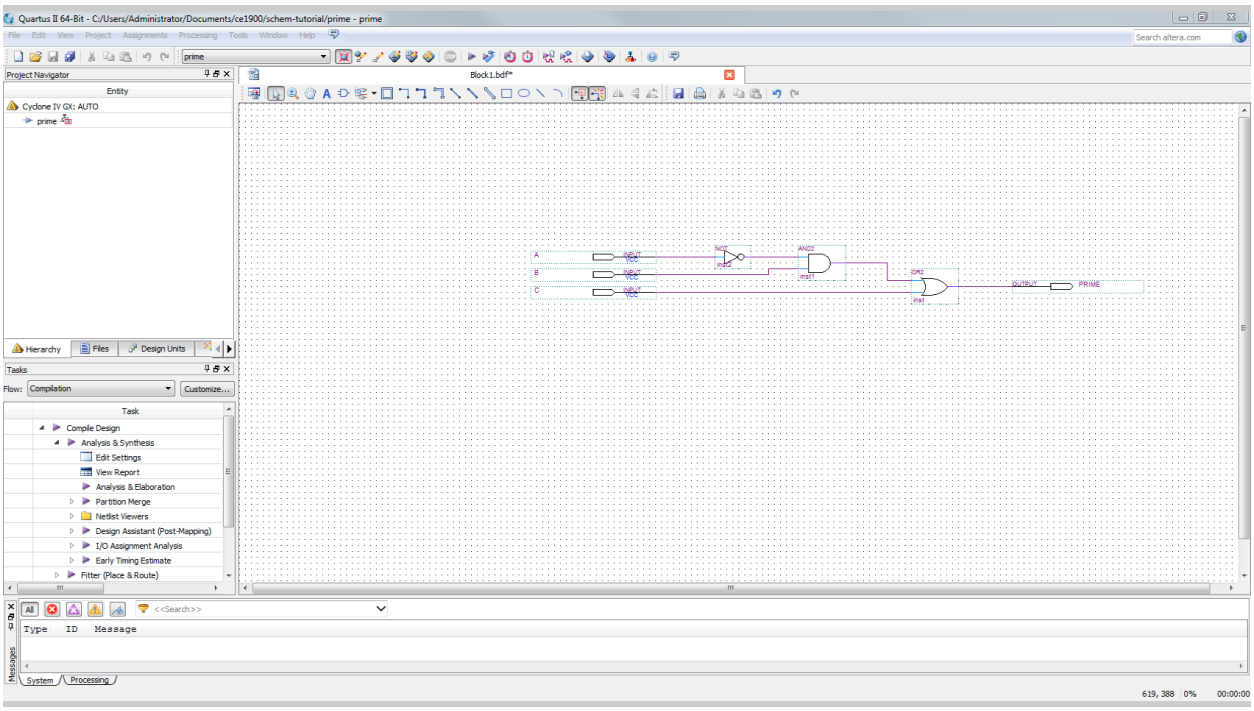
14. **Wire** the components together by clicking and dragging between pins.



Corners can be made by clicking as you drag the mouse.

Drawing blueprints is fundamental in engineering. It's sort of an art form! Your blueprint doesn't have to look exactly like the one shown. Your signal wires might bend earlier or remain straight for that matter. But, the signal wires and gates must be connected together as shown in order to guarantee that electricity flows correctly for the design problem.

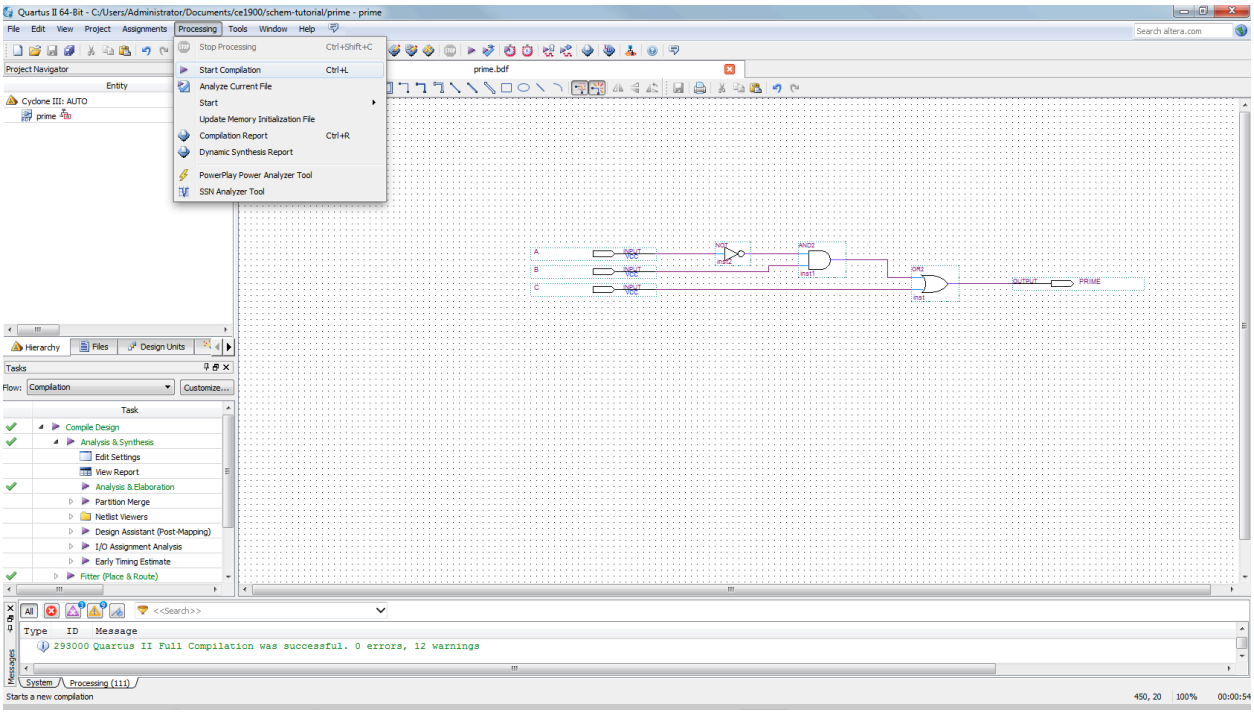
15. **Name** the inputs and outputs by **double-clicking** each one and typing its name.



16. **Save** the completed schematic.

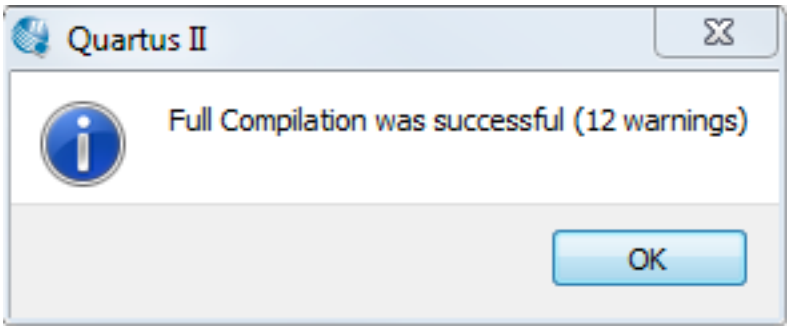
> Use CTRL-S or the "Save" icon. Note that Quartus will present a "Save As" dialog box in the project folder with a pre-assigned name of "prime". Just select the "Save" button.

17. **Compile** the design to check for errors in wire interconnection.
    A. **Choose** “Start Compilation” from the “Processing” menu or just click the “compile” diamond (arrow) just to the right of the gray stop sign icon.
    B. **Note** that the first compilation after software installation may give an error about unlicensed devices. If this happens, **respond** to the error message by choosing Device Family Cyclone III from the Assignments : Devices dialog box. Then try compiling again.



Lots of activity occurs during compilation. Quartus is verifying wire connections, creating a mapping of technologies used in the design, fitting the technology mapping to an automatically chosen integrated circuit chip, creating a programming file for that chip, etc. This process is known as "silicon compilation" or "compile-place-route" in modern digital logic design environments. Keep reading the tutorial to see how you should use the message windows to verify your work.

18. **Wait** patiently while Quartus compiles the design and then **verify** that the compile completed successfully.
    A. **Carefully** check wiring and names if the compiler found errors.
    B. **Recompile** until you achieve successful compilation.



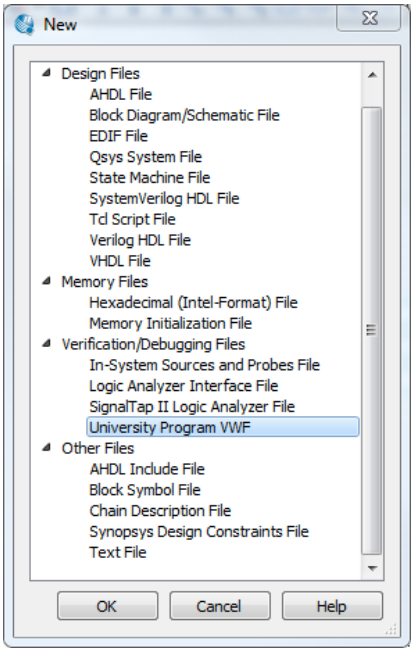
If your dialog box did not say "successful" then you should return to your blueprint and check all of your work.

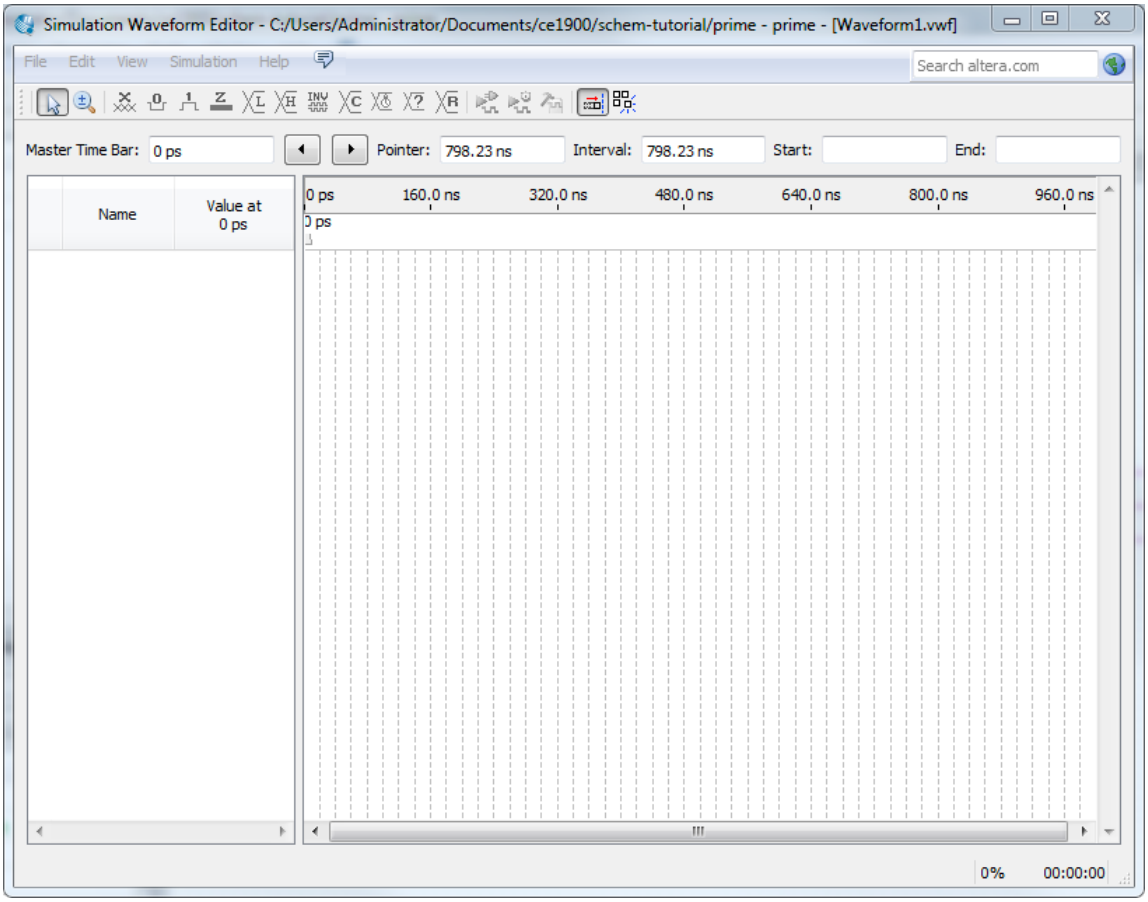
Close the dialog box, of course, when you are done reading it!

19. **Close** the compilation report tab by clicking the tab close box (small X) on the tab.

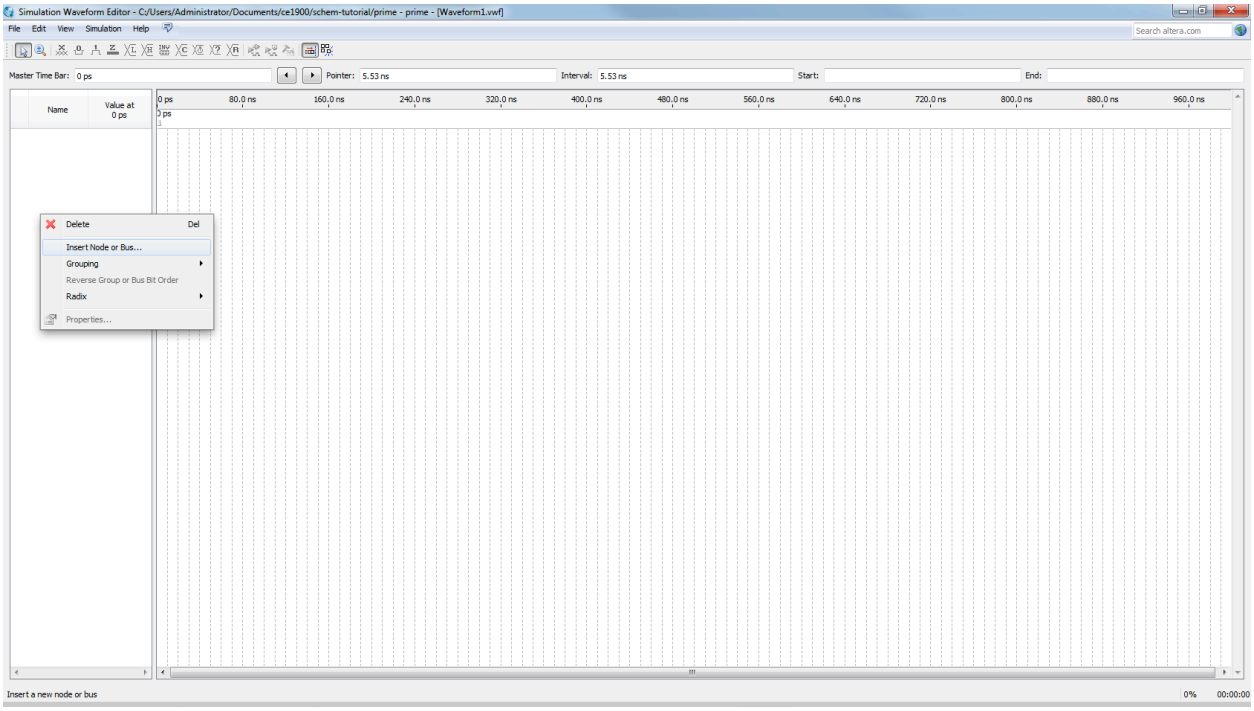
This finishes the basic steps to drop components into a schematic, wire the components together, name inputs and outputs, and complete the compilation of the project to verify connectivity. The next part of the tutorial will explore simulating the circuit to verify correct operation.

20. **Choose** the University Program verification waveform file (VWF) from the File : New dialog box. The simulation waveform diagram editor will open.

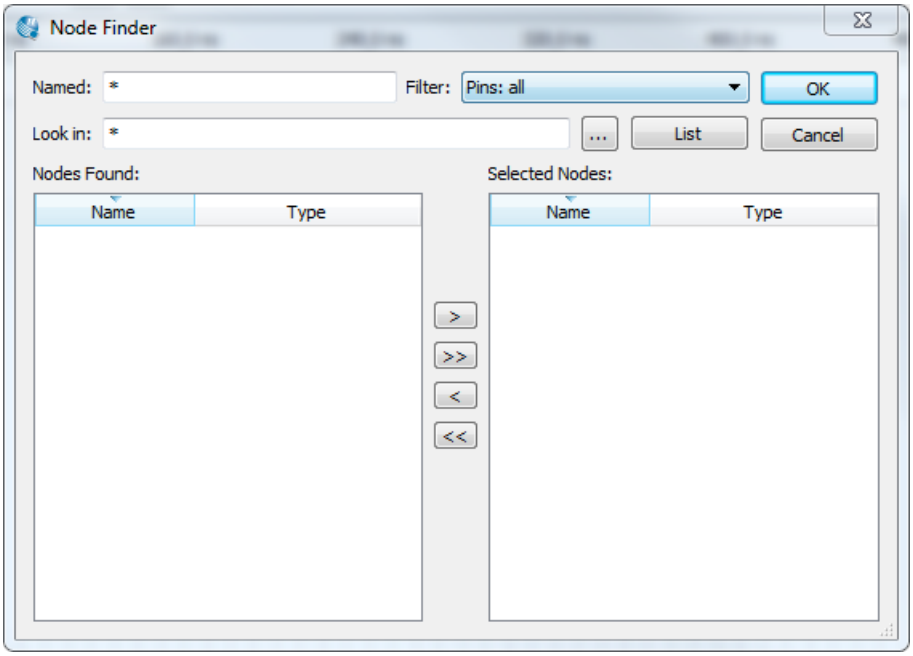




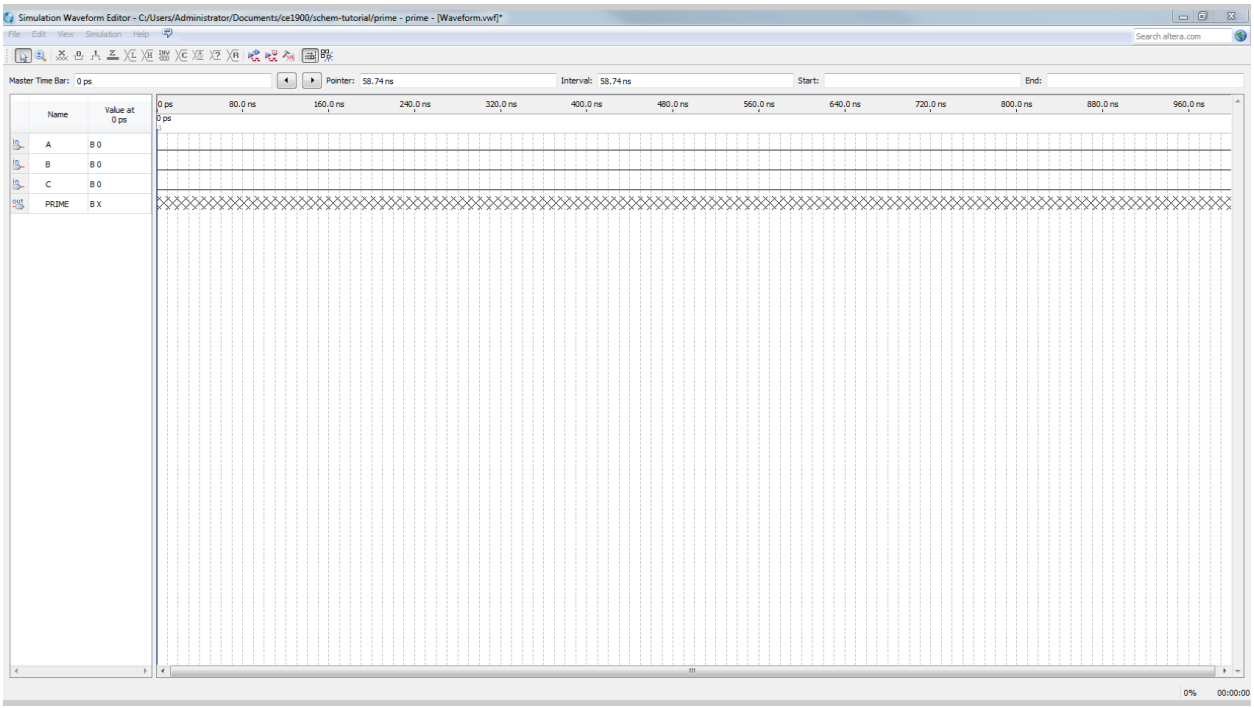
22. Right-click under the “Name” column. Choose “Insert Node or Bus...” from the “Insert” submenu.



23. **Click** the “Node Finder...” button. Quartus calls all pins and gate connections nodes. Thus, all electrical signals are nodes in the circuit. The Node Finder dialog box will open.

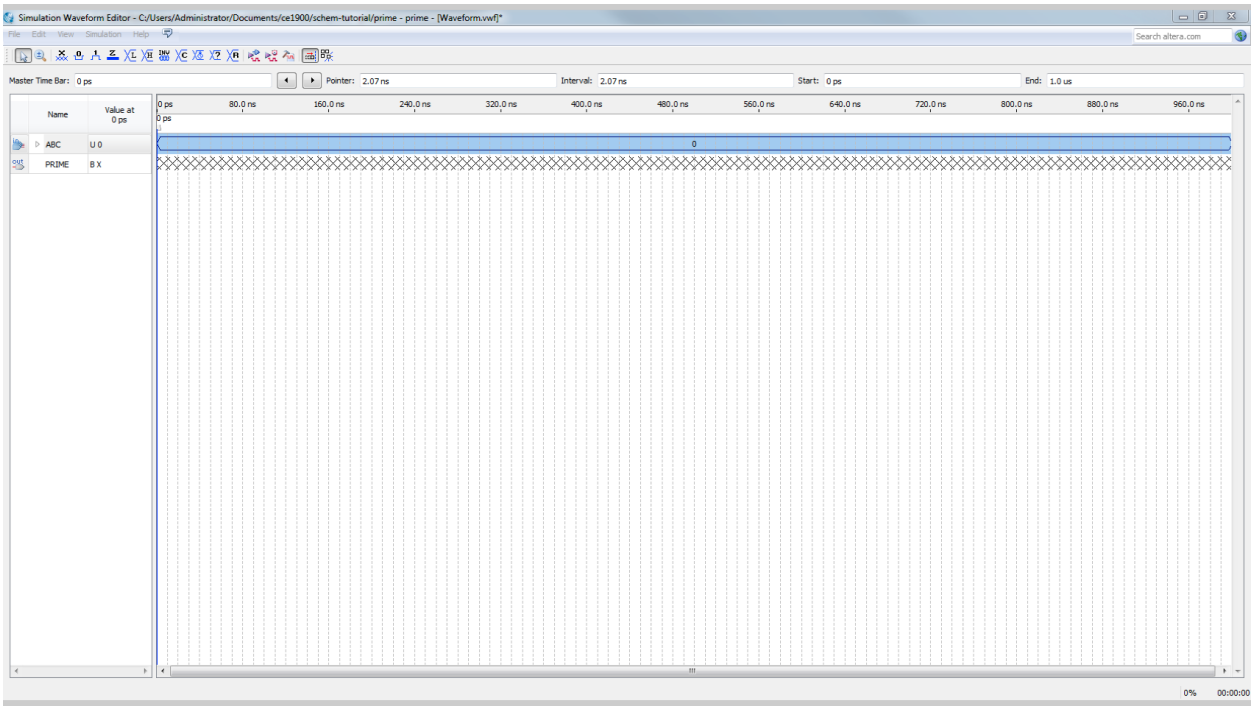


24. **Select** the signals to be presented on the electrical simulation.
    A. **Click** the List button.
    B. **Highlight** all the pins in the left panel and copy them to the right panel – the “selected” panel – by using the copy button “>”. This chooses all the pins as signals of interest for the simulation.
    C. **Click** the OK button to close the dialog box.
    D. **Click** the OK button to close the second dialog box.
    E. **Note** that the waveform workspace panel will now show all the circuit signals with no energy on them. The signal name “PRIME” is shown with “unknown” voltage because it is an output and the simulation has not yet been executed.

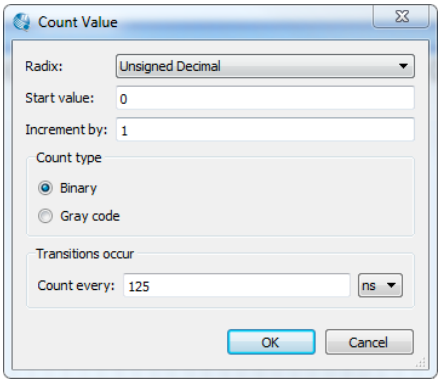


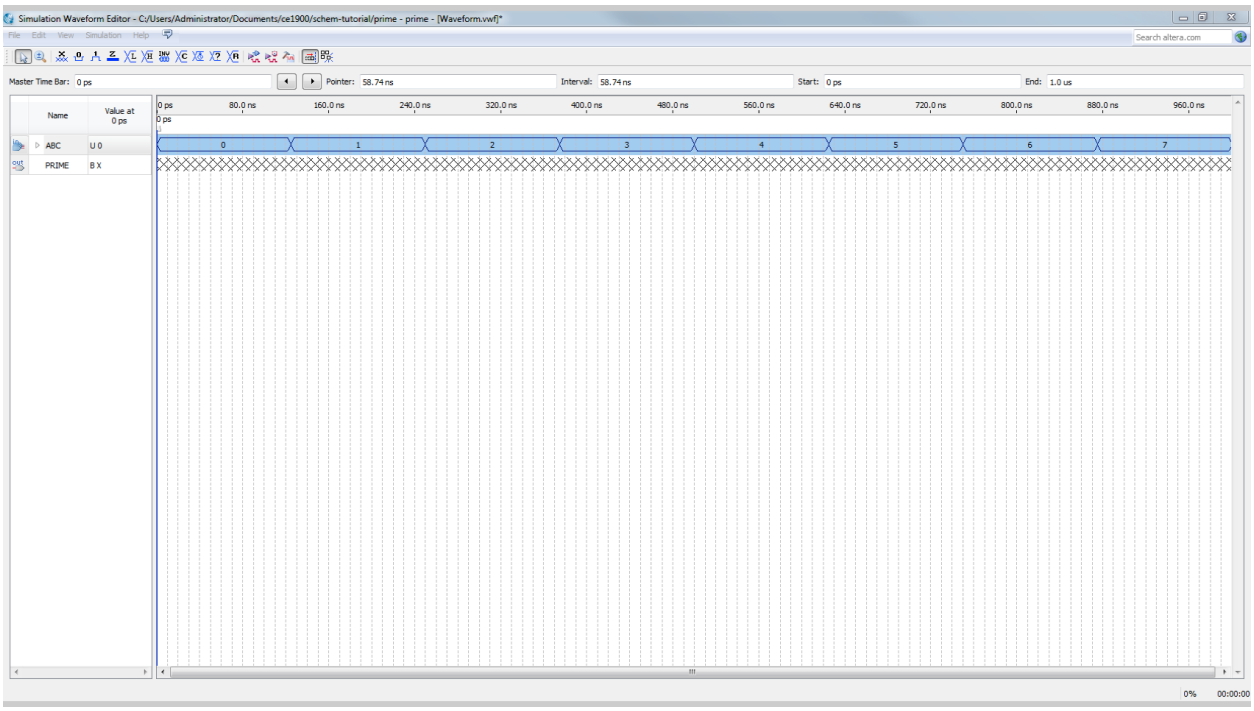
The "Name" sub-panel can be "pulled" to the right using the mouse so that the entire "prime" signal name can be read.

25. **Group** the input bits into a 3-bit binary number.
    A. **Arrange** the signals so that A is at the top of the inputs, B follows, and C is the last input bit.
    B. **Highlight** signals A, B, and C.
    C. **Right-click** on the signal set.
    D. **Choose** Group from the Grouping submenu.
    E. **Note** that grouping allows binary numbers to be written onto the signal group. This is just like signals sitting side-by-side in a truth table.
    F. **Name** the group ABC when asked. Because A is the top signal, it is the most-significant bit and C is the least-significant bit in the group.
    G. **Set** the radix to Unsigned Decimal.
    H. **Close** the Group dialog box.

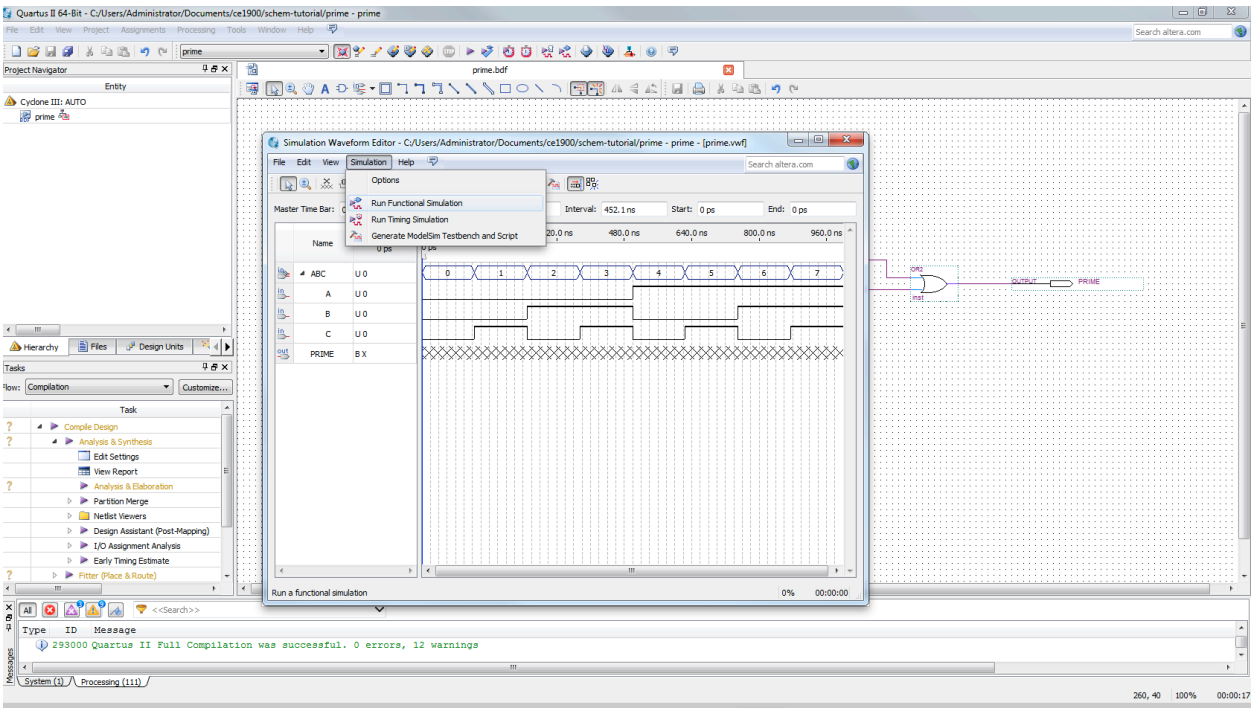


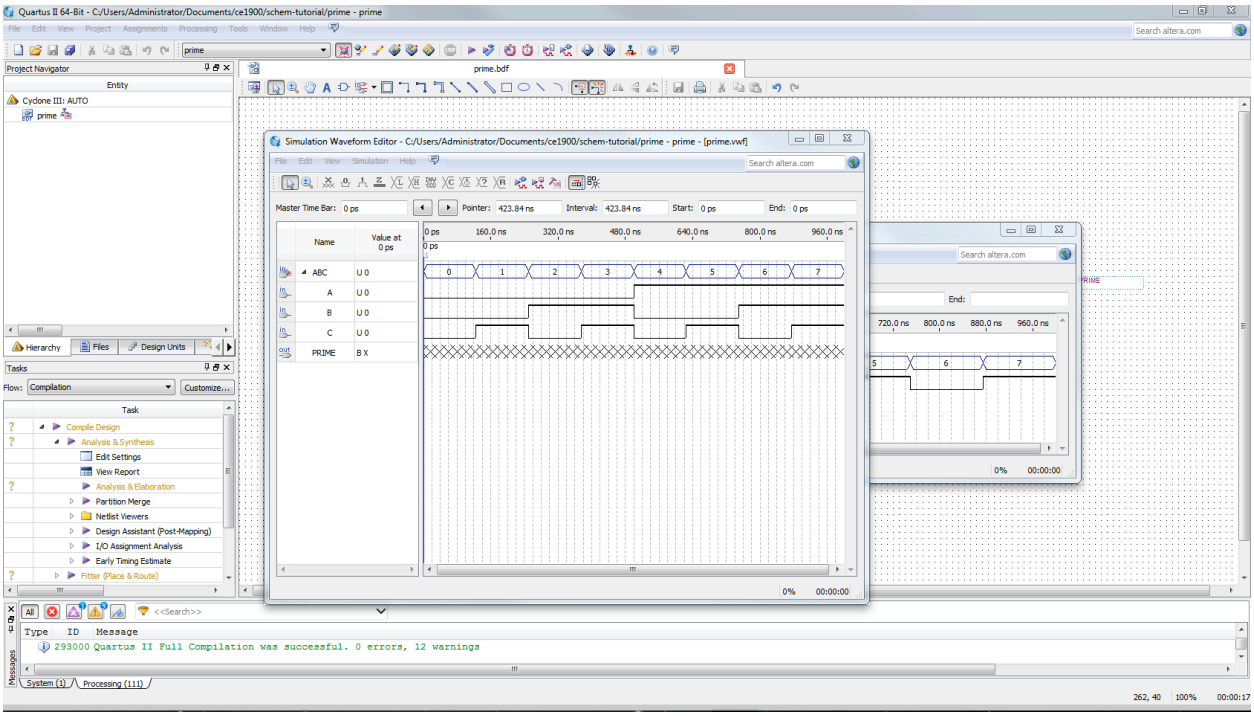
26. **Overwrite** a counting sequence onto the ABC signal group.
    A. **Highlight** the ABC group by clicking its name in the name column.
    B. **Choose** the counting sequence icon from the tool bar. It has a C on it!
    C. **Note** that the simulation window shows 1000 nanoseconds of time. Three binary input signals can encode the numbers 0 through 7 for a total of eight possible inputs. Good simulation practice would examine the PRIME result for each of these possible inputs exactly once. Thus, 1000 ns divided by 8 possible input patterns gives 125 ns of time per input pattern.
    D. **Set** the Count Every entry box to 125 ns. **Read item c** above for an explanation of this number.
    E. **Click** the OK button.





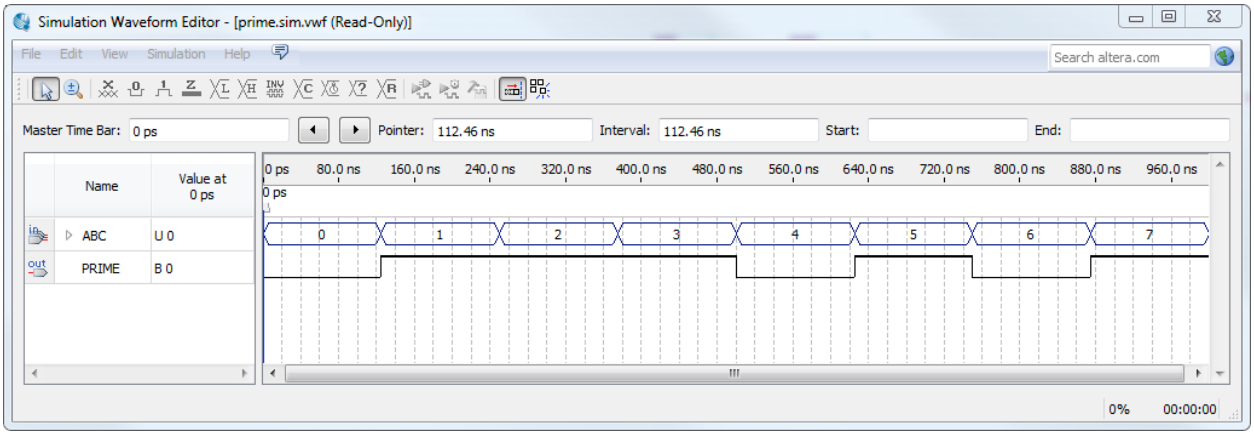
27. **Choose** Run Functional Simulation from the Simulation Menu.
    A. **Name** the waveform file PRIME if asked by the Save dialog box.
    B. **Significant** work will appear on your screen as Quartus simulates.





NOTE THAT THE SIMULATION RESULT WINDOW OPENS BEHIND THE SIMULATION WAVEFORM EDITOR WINDOW

28. **Verify** that the PRIME output signal has energy for every prime number.



29. **Close** the simulator by **clicking** the close (X) icons in the simulator waveform editor and results windows.

30. **Close** the Quartus project by **choosing** Close Project from the Quartus File menu.

This concludes the Quartus schematic and simulation tutorial. **Quit** Quartus using by **choosing** Exit from the File menu.