CE1901 HOMEWORK SET 5

ASSIGNED PROBLEMS

1. **Design** the K-map minimized SOP and POS circuit equations for F(XYZ) = ΠM(6,7). **Analyze** the equations to determine the number of transistors required to implement each circuit. **State** the better choice.
2. The logic gates NOT, AND, and OR are functionally complete. This means that any function can be created using circuits of NOT, AND, and OR gates. Multiplexers are functional level components that are also functionally complete. **Repeat** problem 1 using an 8:1 multiplexer. **Draw** the circuit schematic on paper. **Show** connections between the data inputs and power rails (VCC, GND). **Show** connections between input variables XYZ and selection control signals S2 through S0. **Ensure** your work includes input and output pin symbols.
3. Implement an 8:1 MUX solution to F(XYZ) = $\sum$m(0,1,4,5) using a 74151 multiplexer.
   a. **Review** the data sheet on the course website. Pay close attention to the 74151 IEEE Std. 91-1984 schematic symbol as well as the 74151 truth table. **Note** that the 74151 names its selection control signals C, B, and A rather than S2, S1, and S0. **Note** that bit C is the most significant bit in the truth table. **Finally note** that the 74151 also has an enable control input called G.
   b. **Complete** Quartus schematic and simulation. **Note** you can type 74151 into the part selection box. **Note** that you can type "GND" and "VCC" into the part selection box. **If you get an "inst names already exists" error when compiling**, double click the GND and VCC symbols and change their inst numbers to inst99 and inst98 for example.