CE1901 HOMEWORK SET 6

INSTRUCTIONS

- **Work** these homework problems by yourself on three-hole punched engineering problems paper. Engineering problems paper can be purchased at the MSOE bookstore. Some companies call engineering problems paper an "engineering pad." It is usually green or yellow in color. **Use** the graph paper side **only when drawing graphs**.
- **Do not use calculators** as you work your solutions.
- **Show all work** to receive partial credit.
- **Showing work** means that you illustrate the process you take to complete a problem.
- **Print and three-hole punch** Quartus VHDL, RTL, and simulation waveform diagrams.
- **Print and three-hole punch** this coversheet.
- **Staple** all materials together your solution packet.
- **Submit** your paper solution packet at the start of the **second lecture of week 7**.

ASSIGNED PROBLEMS

1. **Given** a 4-bit bus called H with signals H3, H2, H1, and H0, **use** a K-map to minimize the function F(H) = $\sum$m(0,2,3,4,5,6,10,11). **Calculate** the gate reduction ratio. **Draw** the gate-level circuit as a Quartus schematic blueprint project. **Simulate** to verify correct operation. **Print** schematic and simulation waveforms as part of your submission packet.
2. **Given** a 3-bit bus called B, **use** the 74151 multiplexer to implement the canonical solution of F(B) = ΠM(1,3,6). **Draw** the circuit as a Quartus schematic blueprint project. **Simulate** to verify correct operation. **Print** schematic and simulation waveforms.
    a. **Review** the data sheet on the course website. Pay close attention to the 74151 IEEE Std. 91-1984 schematic symbol as well as the 74151 truth table. **Note** that the 74151 names its selection control signals C, B, and A rather than S2, S1, and S0. **Note** that bit C is the most significant bit in the truth table. **Finally note** that the 74151 also has an enable control input called G.
    b. **Note** that you can type "GND" and "VCC" into the part selection box. **If you get an "inst names already exists" error when compiling**, double click the GND and VCC symbols and change their inst numbers to inst99 and inst98 for example.

PROBLEMS CONTINUE ONTO THE NEXT PAGE

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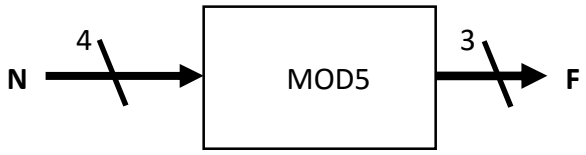
3. A modulo-5 component reports the remainder of dividing an input number N by 5. **Consider** a 4-bit modulo-5 component as shown in the figure. The output = 0 if N / 5 has a remainder of 0. For example, 0/5 = 0 R0, 5/5 = 1 R0. Similarly, the output = 3 if N / 5 has a remainder of 3. For example, 3/5 = 0 R3 and 8/5 = 1 R3. **Create** the truth table. **Implement** the modulo-5 component in Quartus as a VHDL with-select project. **Simulate** to verify correct operation. **Print** VHDL, RTL, and simulation waveforms.



4. Integer division is division that ignores remainder. All digits behind the decimal point are discarded. In other words, decimal point division reports 4/2 = 2.0 and 4/3 = 1.33. In integer division, 4/2 = 2 and 4/3 = 1. Similarly, in integer division, 6/2 = 3 and 7/2 = 3. **Consider** an IDIV4 component that completes integer division-by-4 on a 4-bit input using a VHDL with-select architecture. (Think about the maximum 4-bit input value 15. What is the maximum output? Well, 15/4 = 3.75 = 3 in integer division. Thus, the maximum output is 3 and a 2-bit output bus is required.) **Create** the truth table. **Implement** the IDIV4 component in Quartus as a VHDL with-select project. **Simulate** to verify correct operation. **Print** VHDL, RTL, and simulation waveforms.