

DOWNLOADING DESIGNS TO THE ALTERA DE10-LITE FPGA

Consider the design of a three-bit prime number detector completed in the MSOE schematic entry tutorial. Figure 1 shows the block diagram and truth table. The inputs are binary signals A, B, and C while the output is binary signal PRIME. Note that this example calls one (001) a prime number for the purposes of illustrating equation simplification. The mathematical definition of a prime number would not consider one as prime.

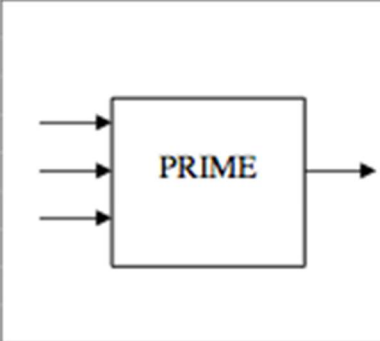
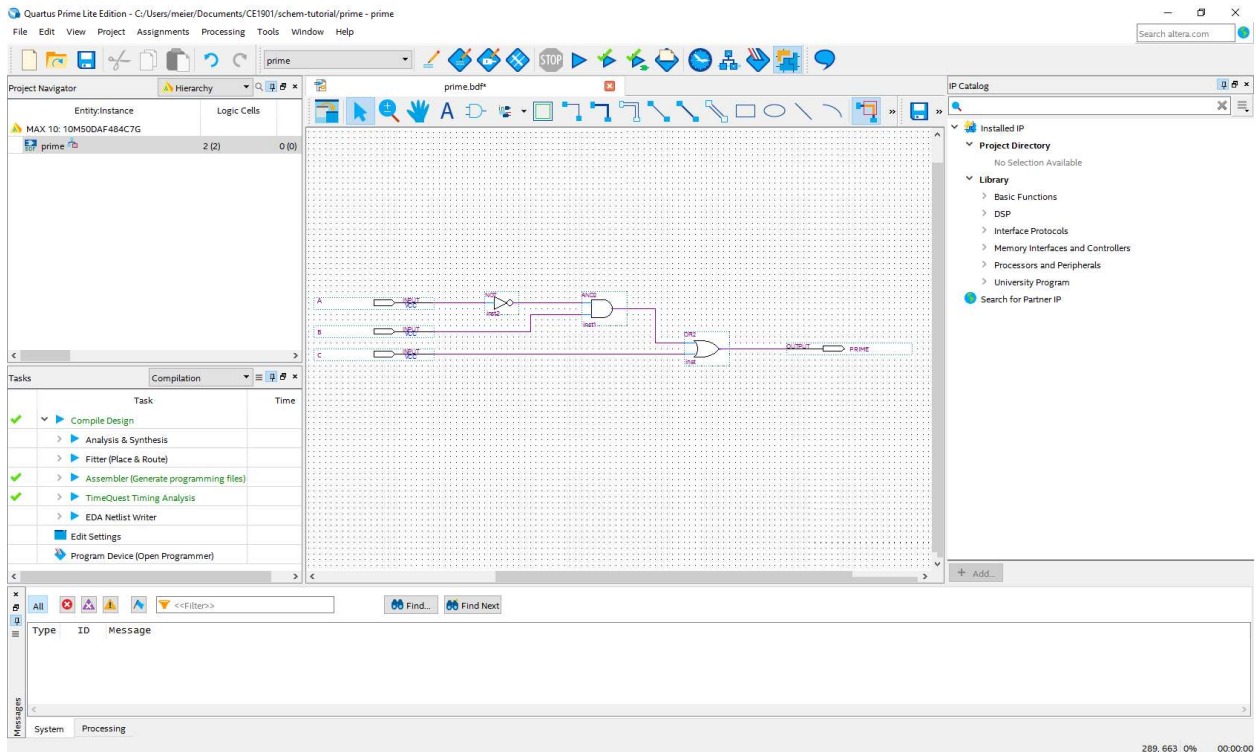
	A	B	C	PRIME
	0	0	0	0
	0	0	1	1
	0	1	0	1
	0	1	1	1
	1	0	0	0
	1	0	1	1
	1	1	0	0
	1	1	1	1

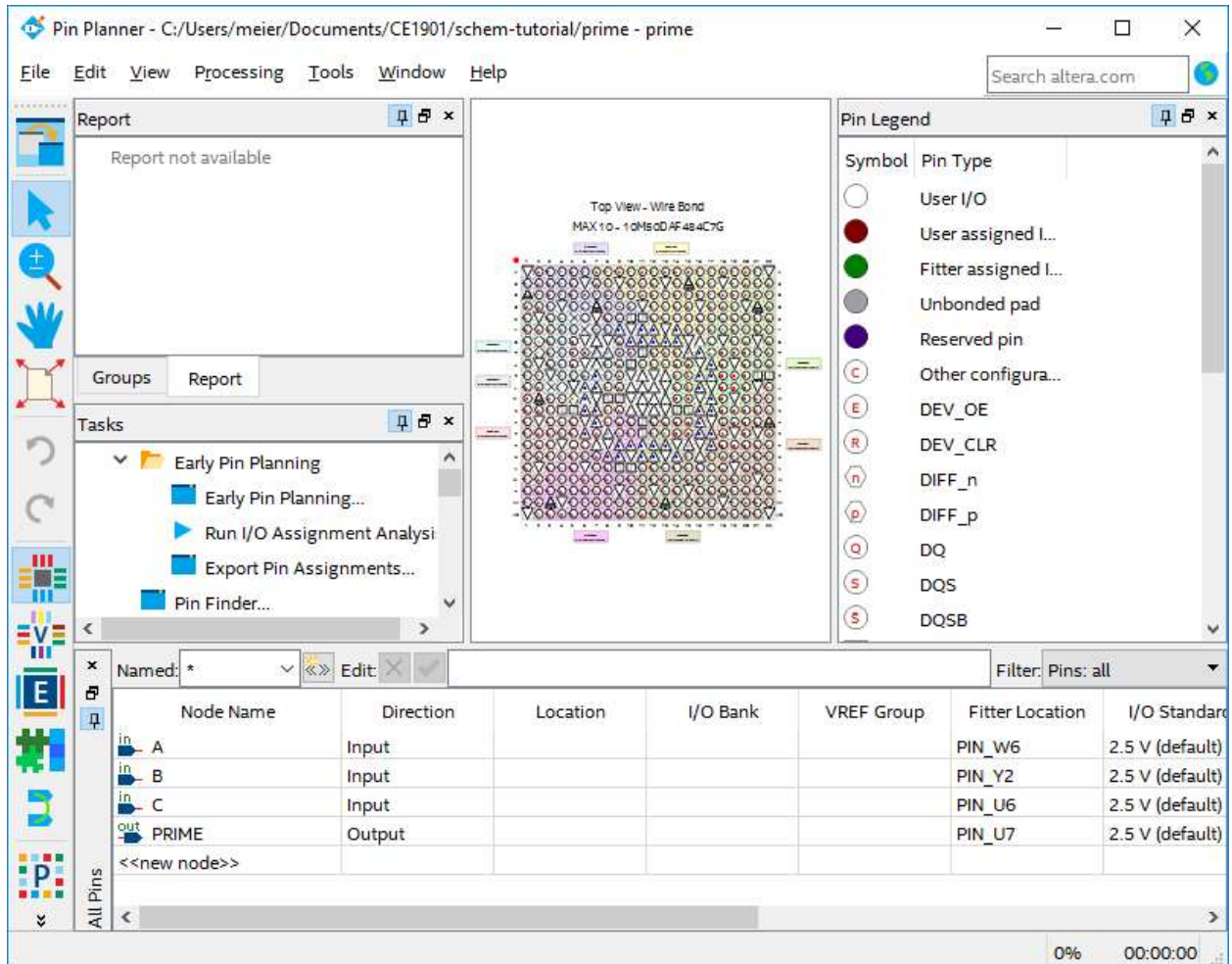
Figure 1: A Prime Number Detector

This tutorial assumes that you have completed the MSOE schematic entry tutorial, that the correct chip was selected at project creation, and that the design compiles without error.

1. **Start** Quartus and open your completed DE10-Lite design project.
 - a. **Use** File → Open Project and browse to your schematic tutorial directory.
 - b. **Choose** the “prime” QPF file. **Hoover** over each icon in your file browser and after a couple of seconds Windows will show you the file type.
 - c. **Double-click** the “prime” schematic file in the Project Navigator pane on the left hand side of the screen to re-open the schematic diagram.



2. **Choose** the Pin Planner from the Assignments menu.



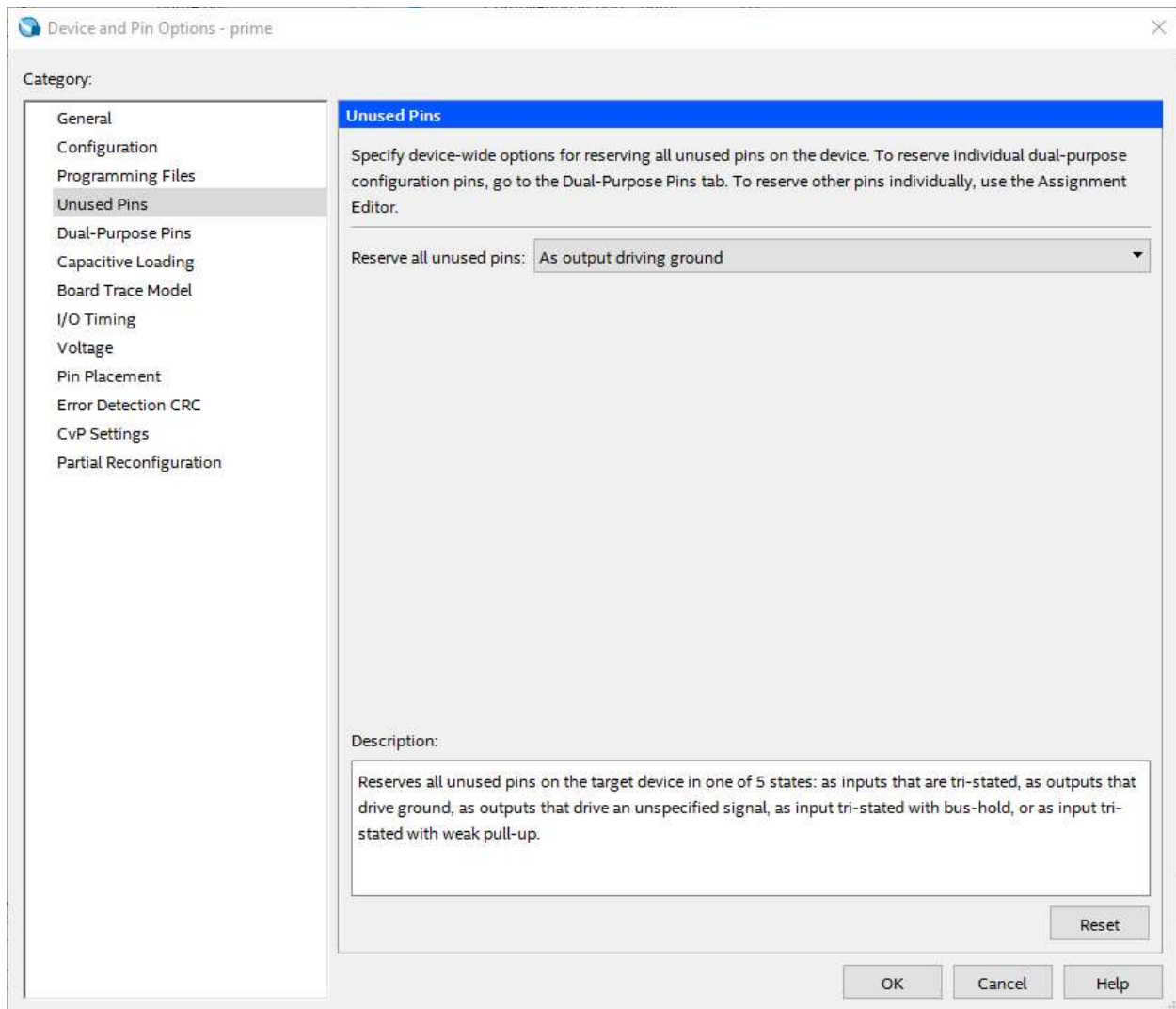
3. **Assign** signals to appropriate DE10-Lite pins. **Consult** the umannual available on your course website for available input and output devices. This example uses three slide switches as inputs A,B,C mapping A to switch SW2, B to switch SW1 and C to switch SW0. Silkscreen print above the switches on the DE10-Lite help you identify switches by name. Figure 3-15 in the user manual shows the connections between switches and Altera MAX 10 chip pins. The PRIME output drives energy onto LEDR0. **Type** the alphanumeric D12 in the “Location” field for input A. **Repeat** for each input and output pin using the assignments given in this table.

SIGNAL NAME	USER MANUAL REFERENCE	DE0-Nano-SOC PIN
A	Reference Figure 3-15	D12
B	Reference Figure 3-15	C11
C	Reference Figure 3-15	C10
PRIME	Reference Figure 3-16	A8

Node Name	Direction	Location	I/O Bank	VREF Group	Fitter Location	I/O Standard
in A	Input	PIN_D12	7	B7_NO	PIN_W6	2.5 V (default)
in B	Input	PIN_C11	7	B7_NO	PIN_Y2	2.5 V (default)
in C	Input	PIN_C10	7	B7_NO	PIN_U6	2.5 V (default)
out PRIME	Output	PIN_A8	7	B7_NO	PIN_U7	2.5 V (default)
<<new node>>						

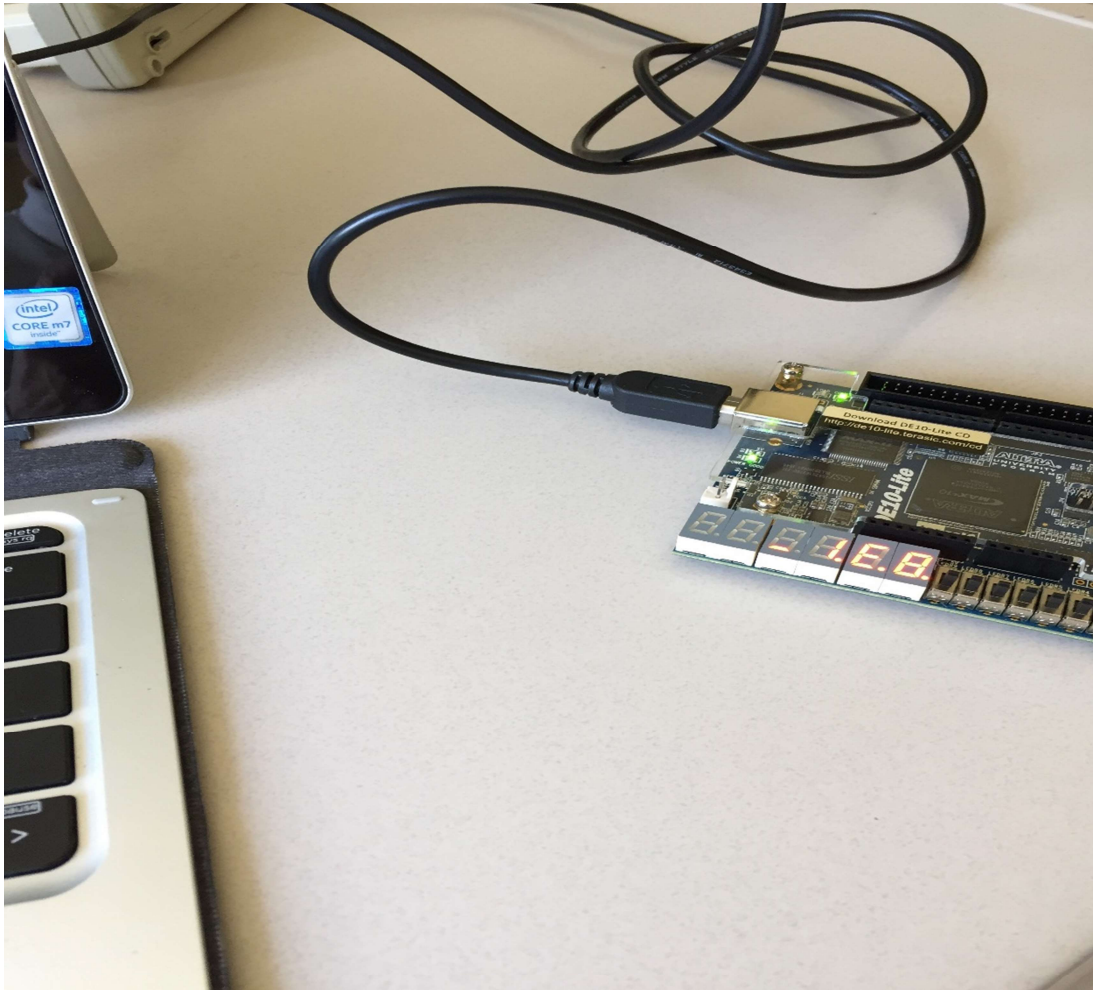
4. **Close** the Pin Planner.

5. **Assign** behavior for all unused pins on the chip. **Choose** Add Device... from the Assignments menu. **Click** the Device and Pin Options... button. **Set** Unused Pins to outputs driving ground. **Click** the OK buttons to close the dialogue boxes.

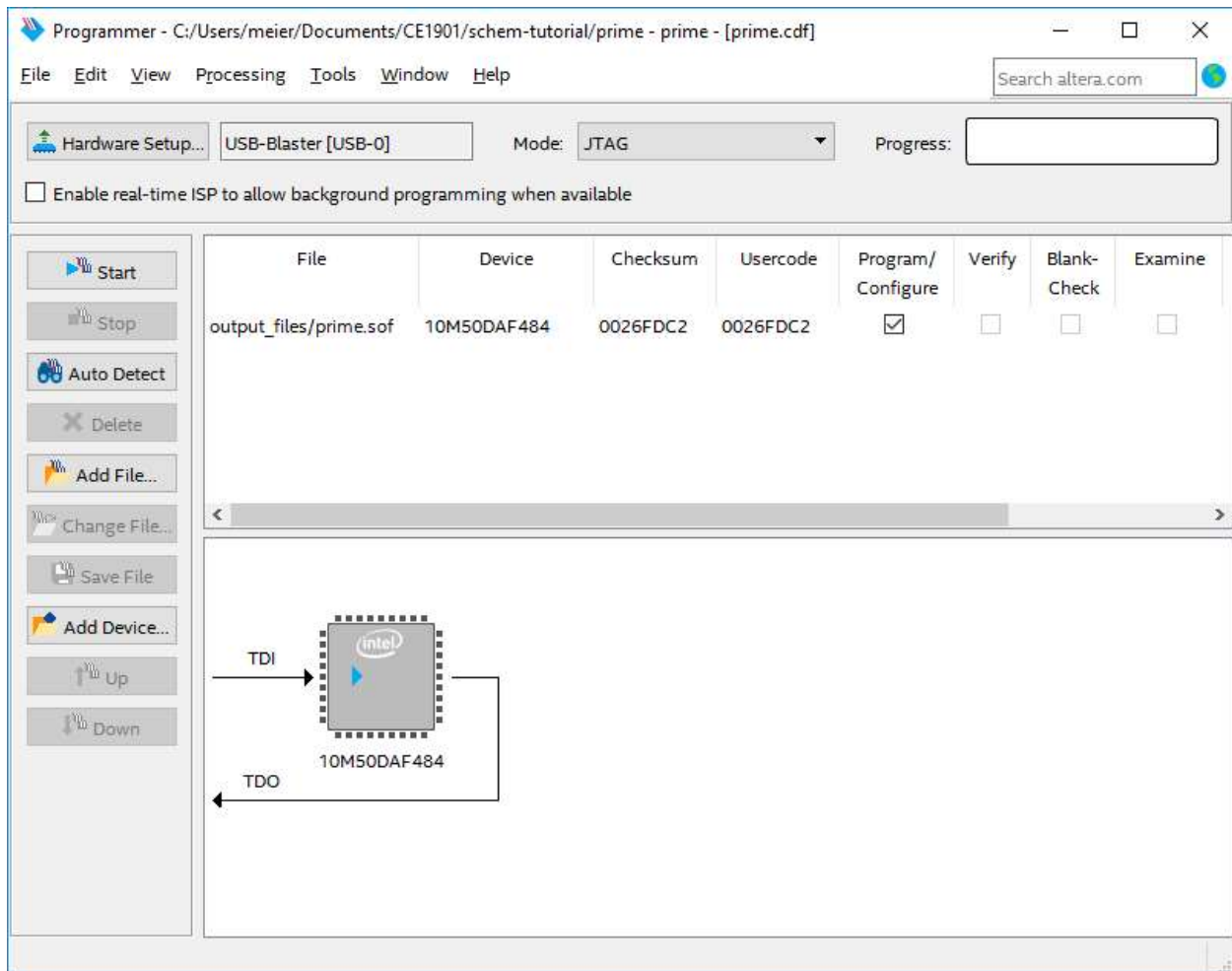


6. **Recompile** the design by choosing the “compile” arrow just to the right of the gray STOP icon in the toolbar.

7. **Connect** the DE10-Lite to a USB port.



7. **Click** the Programmer toolbar icon. You can also use Tools → Programmer. This will open the Programmer dialog box.



- **Ensure** that the DE10-Lite USB-Blaster is selected as the dialogue box opens. **Use** the Hardware Setup button if it is not automatically selected. **See** the last page of this document if no hardware is visible under Hardware Setup.
- **Ensure** that the 10M50DAF484 chip is automatically detected as the dialogue box opens. **Use** the Auto Detect button if it is not automatically detected.
- **Ensure** the SRAM Object File (sof) for the project is added to the programmer file window as the dialogue box opens. **Use** the Add File button if it is not automatically added.
- **Ensure** the Program/Configure checkbox is checked.
- **Click** the **Start** button to blast your configuration file into the MAX10 chip.

14. **Verify** your design works by adjusting the slider switches to difference binary numbers and monitoring the PRIME light.
15. **Close** the programmer dialog box and Quartus. This completes the FPGA programming tutorial.

This diagram shows the complete Quartus Build-Simulate-Test design flow.



DEVICE DRIVER INSTALLATION PROBLEMS

The USB-Blaster device driver was part of the Software Center install. Sometimes it does not install properly. If no hardware is visible in the Hardware Setup dialogue box then you need to install the drivers. **Use** this process.

1. Search Icon in Windows Toolbar → Device Manager
2. Identify the USB-Blaster under Other Devices.
3. Double-click it.
4. Choose Browse My Computer
5. Choose Browse...
6. Browse to: OSDisk (C:) → intelFPGA_lite → 17.0 → quartus → drivers
7. Highlight usb-blaster
8. Click Next to finish the install.
9. Windows may ask you if you “want to install it”. Ok the install.
10. Return to the programming step and restart your work.