SCHEMATIC DESIGN IN QUARTUS

Consider the design of a three-bit prime number detector. Figure 1 shows the block diagram and truth table. The inputs are binary signals A, B, and C while the output is binary signal PRIME. Note that this example calls one (001) a prime number for the purposes of equation simplification. The mathematical definition of a prime number would not consider one as prime.
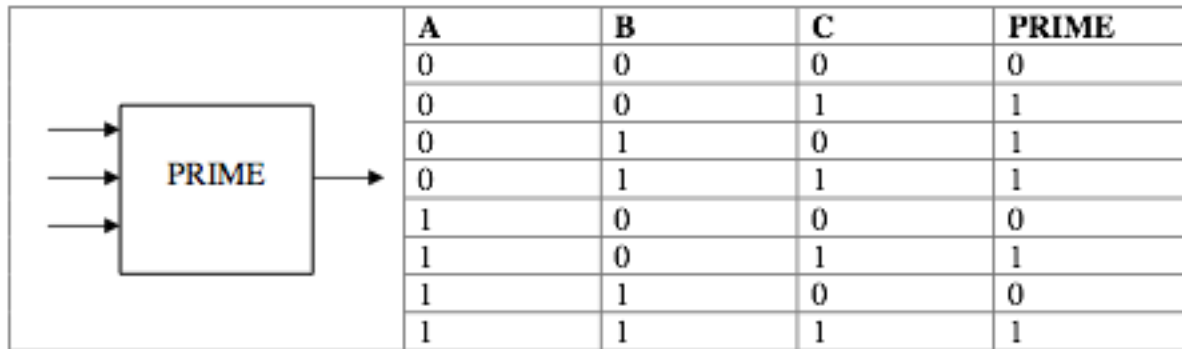
PRIME	A	B	C	PRIME
	0	0	0	0
	0	0	1	1
	0	1	0	1
	0	1	1	1
	1	0	0	0
	1	0	1	1
	1	1	0	0
	1	1	1	1

Figure 1: A Prime Number Detector

This document will illustrate how to create a Quartus schematic project to draw and simulate the prime number detector. Students will likely not understand the derived circuit equations or the schematic diagram early in the quarter when working this tutorial. Students will learn how to complete the design as the quarter progresses.

Note that your Quartus version may present slight differences in the program title bars, dialog box titles, option choices, menus choices, etc. The basic windows do not change from version to version so the original screenshots have been retained for ease of tutorial document maintenance.

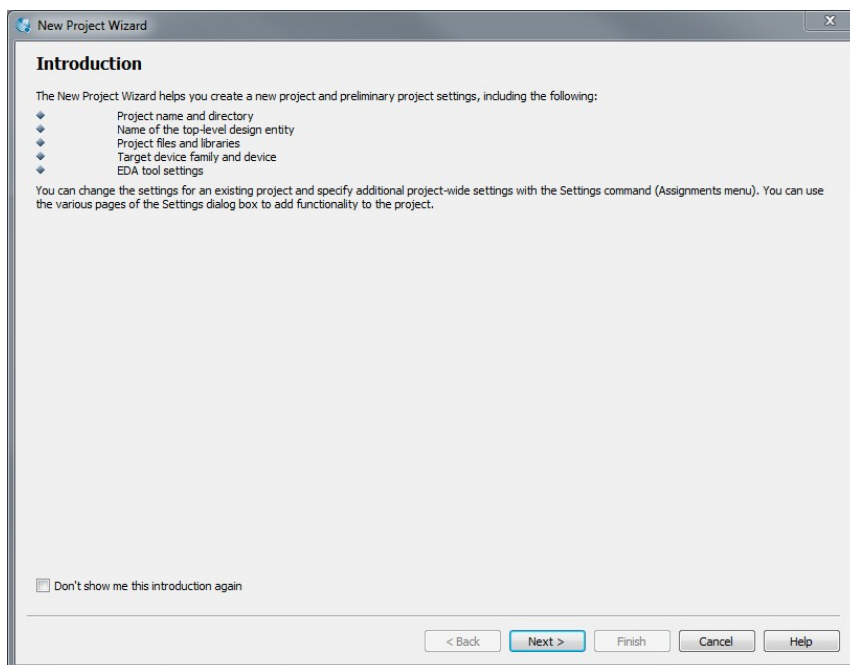1. **Start** Quartus. It will present you with the standard blank startup window.
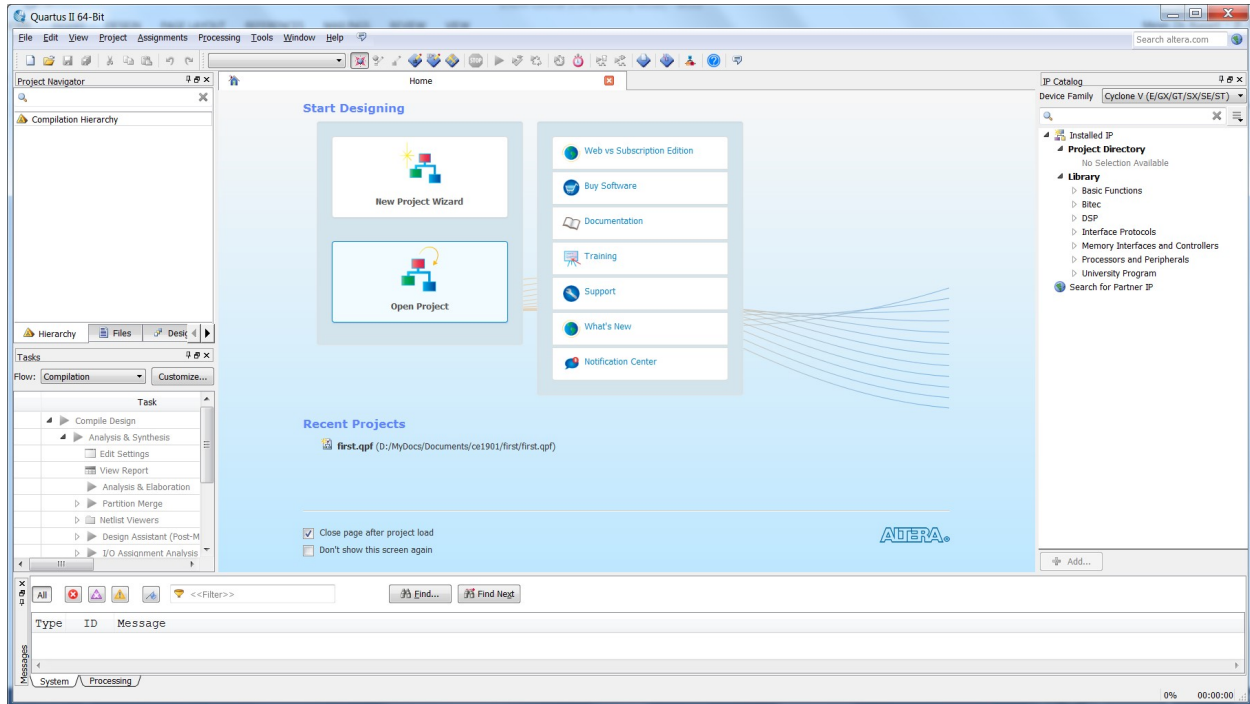
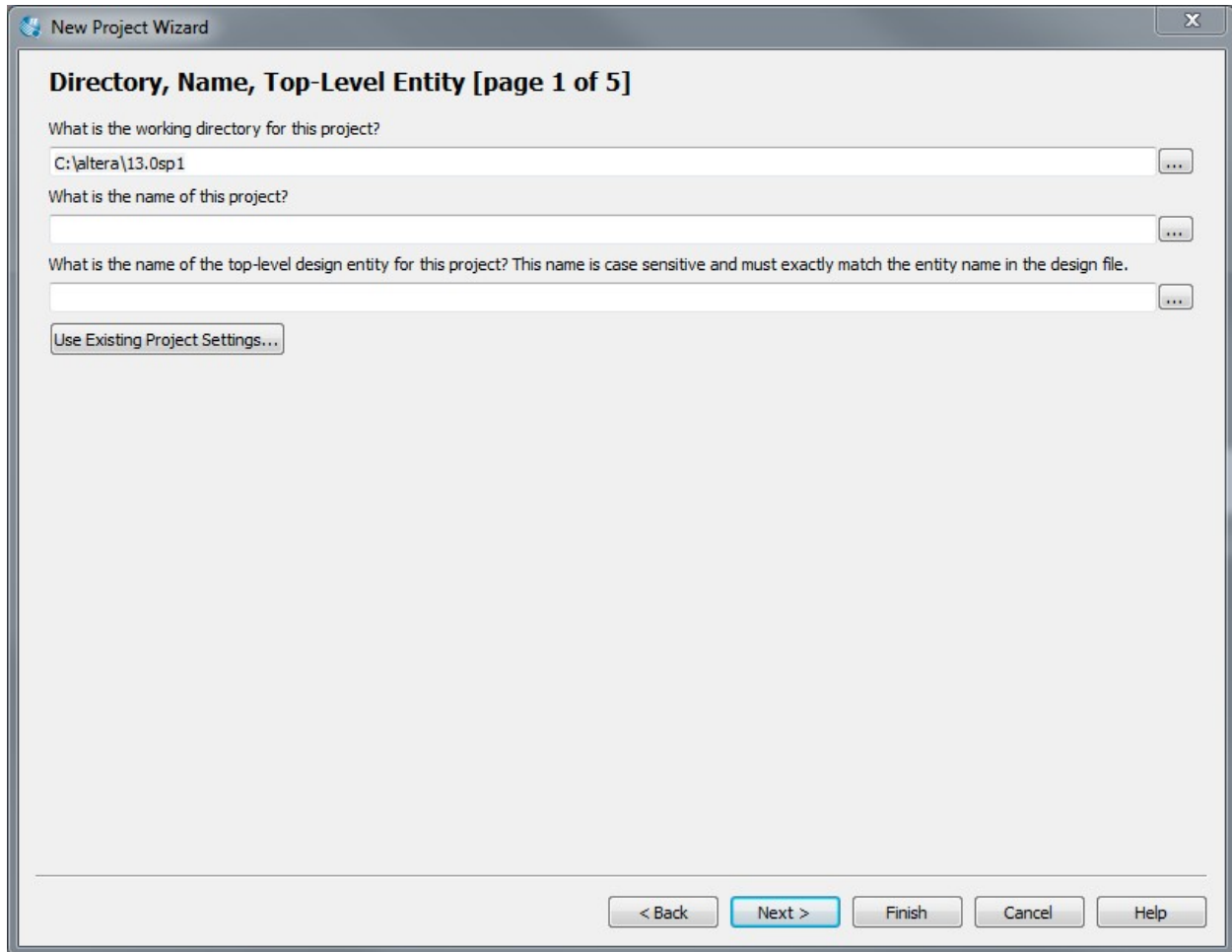**Note** that as Altera updates Quartus this view may change slightly.

2. **Create** a new project for your circuit design by **choosing** "New Project Wizard" from the "File" menu or from the center panel of the startup screen. A project is a collection of files completing the circuit design. Engineers create design files during design. Quartus creates additional design files when processing those created by engineers.


3. Click the "Next" button to advance beyond the information dialog box.

4.	**Click** the "…" button next to the working directory textbox.

New Project Wizard

Directory, Name, Top-Level Entity [page 1 of 5]

What is the working directory for this project?

C:\altera\13.0sp1   [...]

What is the name of this project?

   [...]

What is the name of the top-level design entity for this project? This name is case sensitive and must exactly match the entity name in the design file.

   [...]

[Use Existing Project Settings...]

[< Back] [Next >] [Finish] [Cancel] [Help]

5. **Create** a project folder for your project work.
   A. **Browse** to your Documents folder using the side bar in the file browser.
   B. **Create** a CE1901 folder using the New Folder choice above the side bar.
   C. **Double-click** the CE1901 folder to move inside of it.
   D. **Create** a schematic tutorial folder. This tutorial names the folder as schem-tutorial.
   E. **Double-click** the schem-tutorial folder to move inside of it.
   F. **Choose** Select Folder.
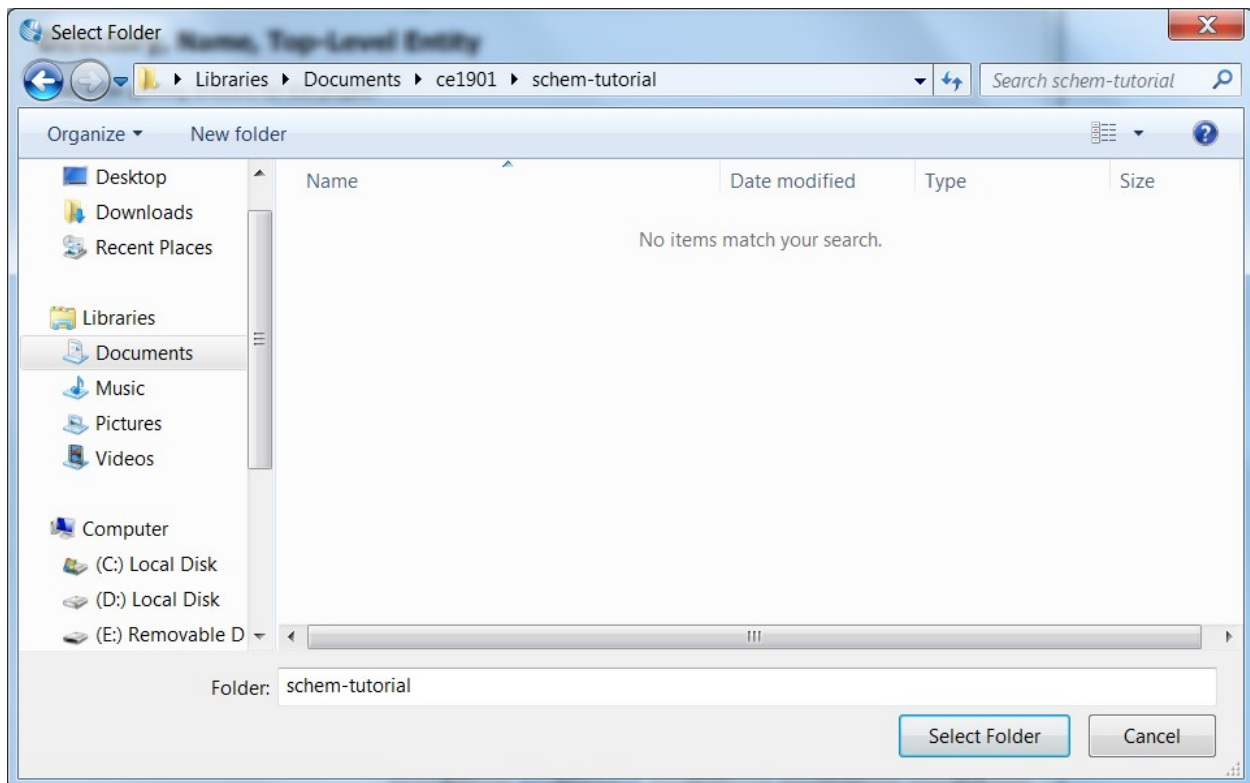
Look closely at the screenshot. The instructors recommend you make a CE1901 folder inside your Documents folder. You will then place project folders inside the CE1901 folder through the rest of the quarter. Good project management is an example of professionalism.

6. **Name** the project and top-level entity "prime". Simple projects with a single functional block – like this one – usually match the project and entity names. More complicated projects may have different names. Examples of this type of project will be seen later in the quarter. **Click** the "Next" button.

New Project Wizard

Directory, Name, Top-Level Entity

What is the working directory for this project?

D:/MyDocs/Documents/ce1901/schem-tutorial

What is the name of this project?

prime

What is the name of the top-level design entity for this project? This name is case sensitive and must exactly match the entity name in the design file.
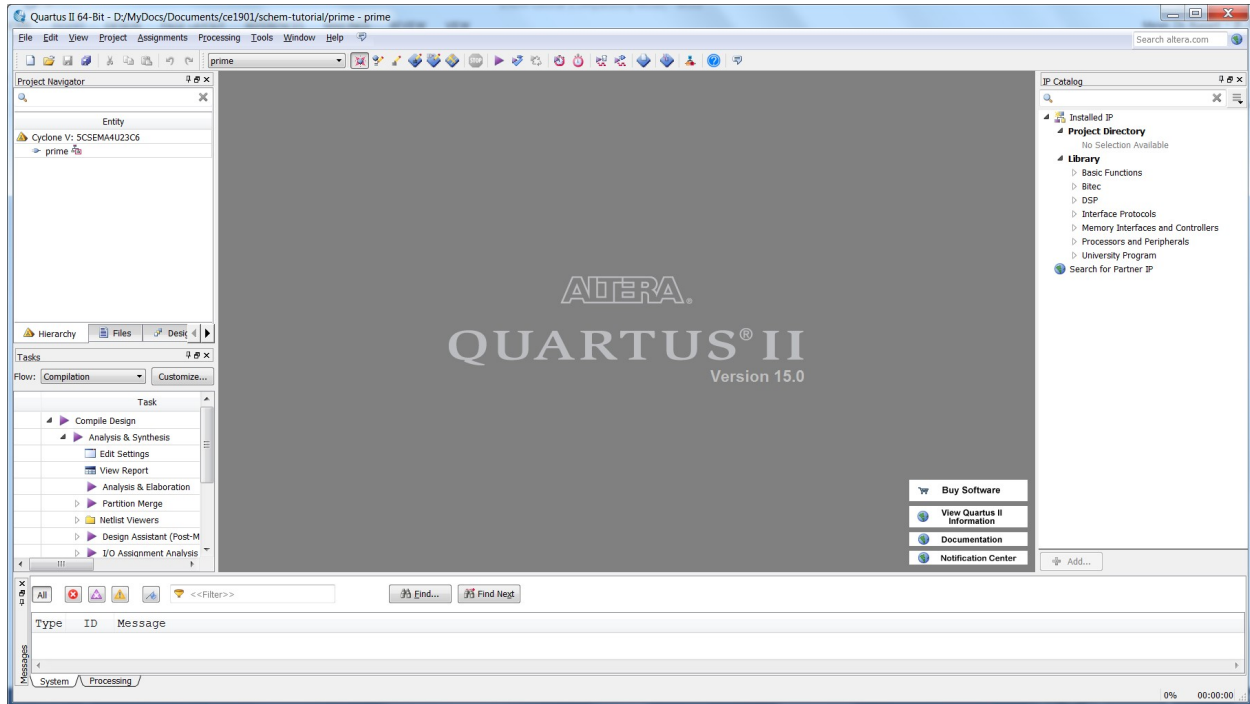
prime

Use Existing Project Settings...

< Back   Next >   Finish   Cancel   Help

7.   **Click** the "Next" button two more times and arrive at the "Family, Device Board Settings" dialog box. This dialog box allows you to choose specific Altera FPGA devices to host your design as hardware components. The DE10-Lite lab board uses an Altera <mark>MAX 10 10M50DAF484C7G</mark>. **Set** the family choice to MAX 10. **Choose** the specific MAX10 device in the scrollable list of devices. A quick way to get to this device is to type 10M50 in the "Name Filter" text box on the right-hand side and then select the correct one in the "Available Devices" panel.
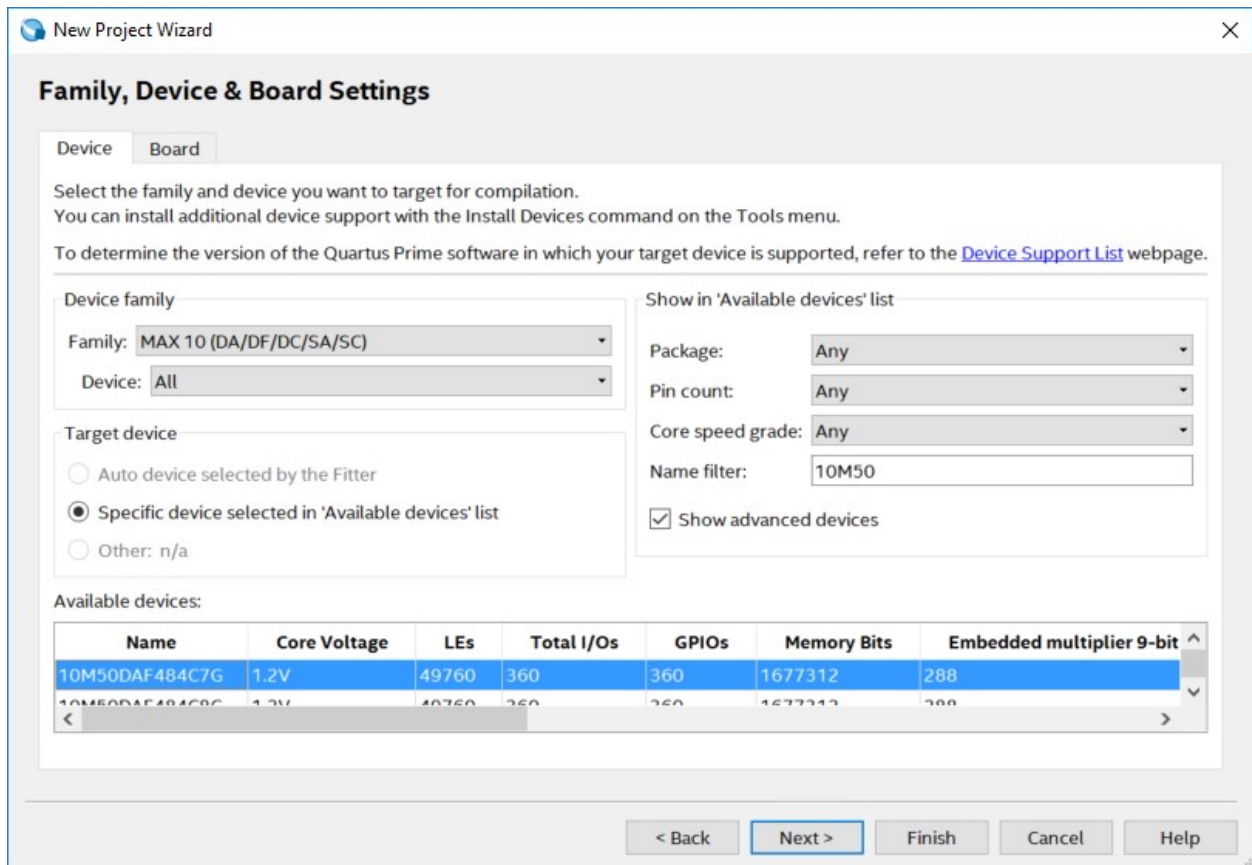

8.   **Click** the "Finish" button.

9.   **Note** the entity file named "prime" in the Project Navigator tab on the left of the screen. You can open the Project Navigator if it is accidentally closed by choosing View:Utility Windows:Project Navigator from the menus.


This screenshot also shows the IP Catalog open on the right hand side of the screen. You can open the IP Catalog if it accidentally closed by using the same process of selection in the View menu.

10. **Add** the schematic diagram for entity prime.
   A.   **Choose** the "new" toolbar icon, the "New..." choice from the "File" menu, or type ctrl-n. The "New" dialog box will appear.
   B.   **Highlight** "Block Diagram/Schematic File".
   C.   **Click** the "OK" button.
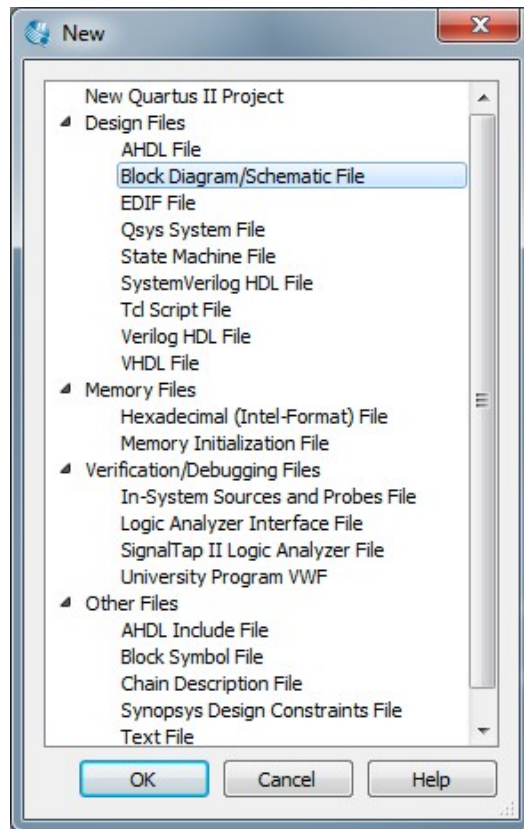
Schematic diagrams are blueprints of digital computer circuits.

11. **Click** the window "Maximize" button to the left of the "X" window close button to bring the schematic size full-screen.
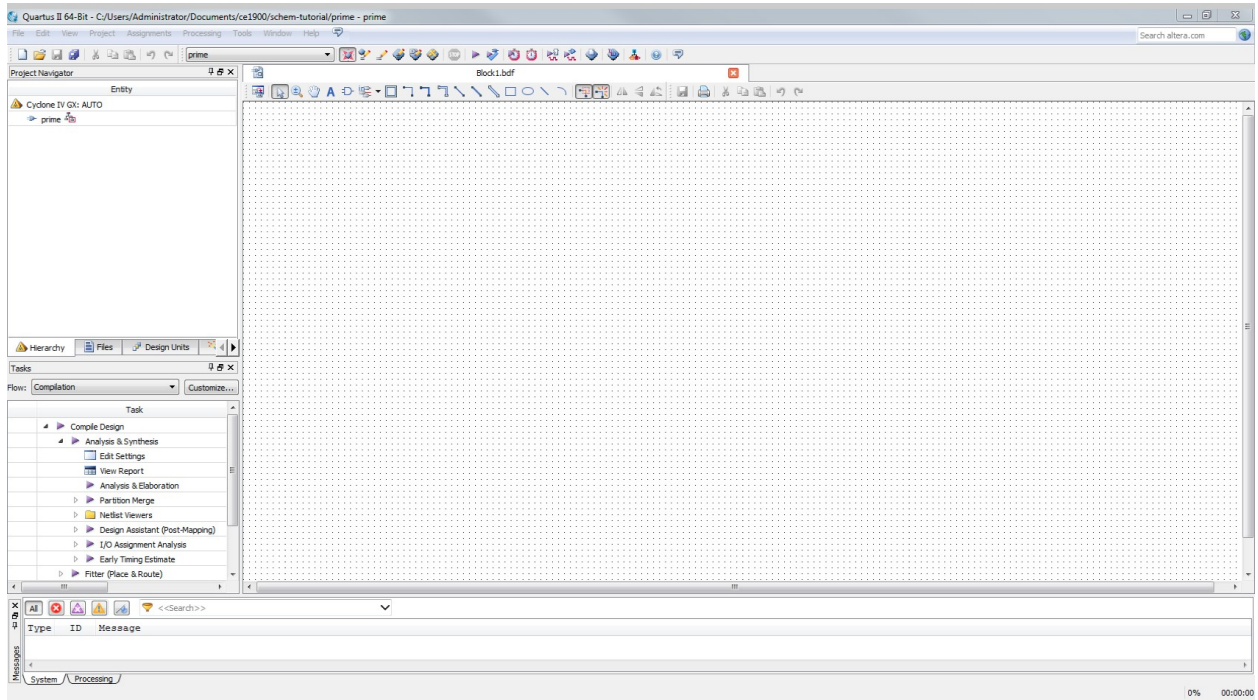
Quartus is a Windows application. You will feel quite comfortable with the menu structure, maximizing, minimizing, saving, and printing.

12. **Double-click** inside the schematic grid to call-up the component library symbol browser.

   A. **Note** that this example has expanded the library to see the basic logic gates.
   B. **Note** that you can also type the name of the component in the "Name" textbox to quickly locate it.
   C. **Select** the 2-input OR gate (OR2) to get started building the minimized equation for function PRIME. **Click** Ok.
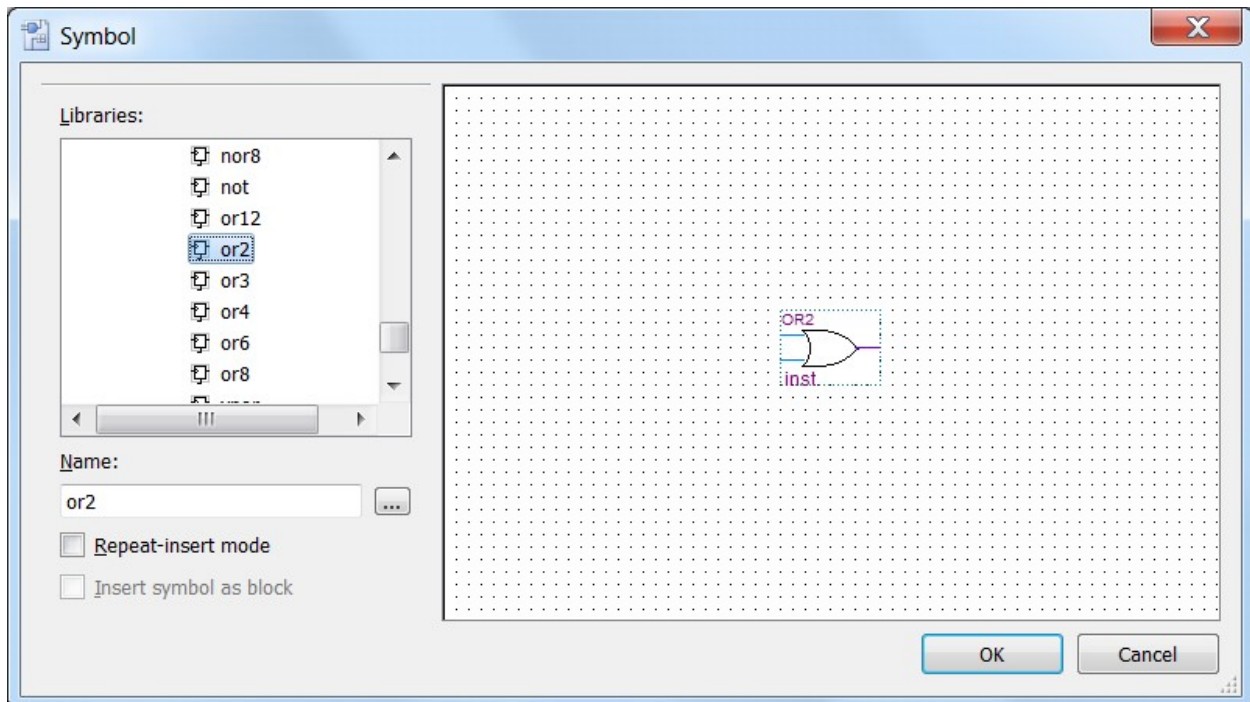

Boolean Equations for PRIME:

The canonical equation is: PRIME=$\sum$m(1,2,3,5,7)=A'B'C+A'BC'+A'BC+AB'C+ABC
The minimized equation is: PRIME=A'B+C

You will be able to derive these equations by weeks 3 and 4 of the quarter. Remember to come back and try to match these equations then!

13. **Place** the OR2 component toward the right-hand side of the schematic by rolling the mouse into position and clicking the mouse button.
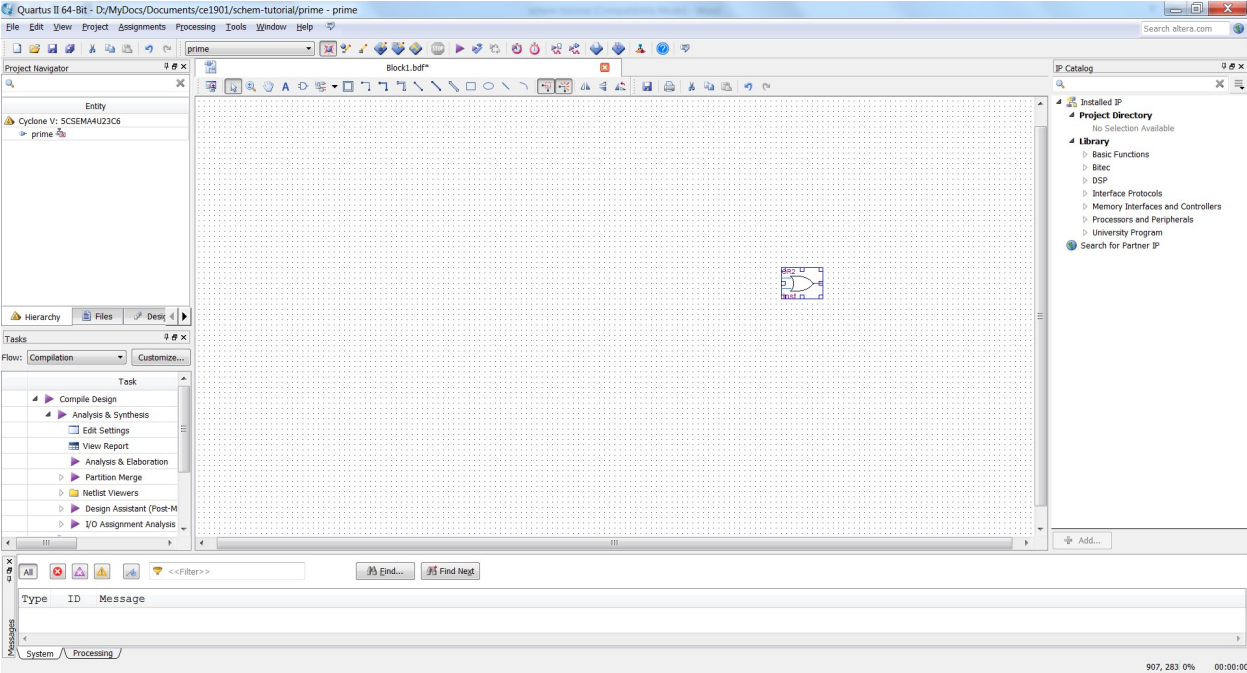
14. **Place** an AND2 component, a NOT component, three input components, and one output component. **Use** the name field in the library dialog box to make finding each component easy. The standard component names are: AND2, input, output.
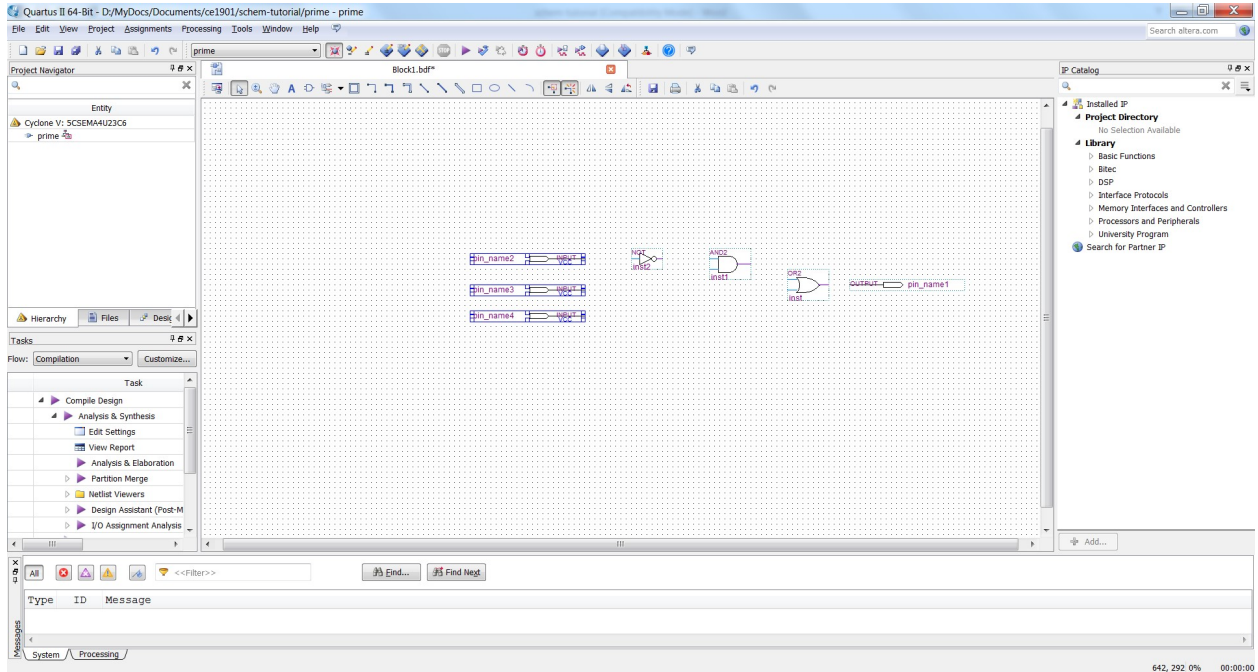
Remember that you can get to the library by "double-clicking" in blank space on the schematic.

15. **Wire** the components together by clicking and dragging between pins.
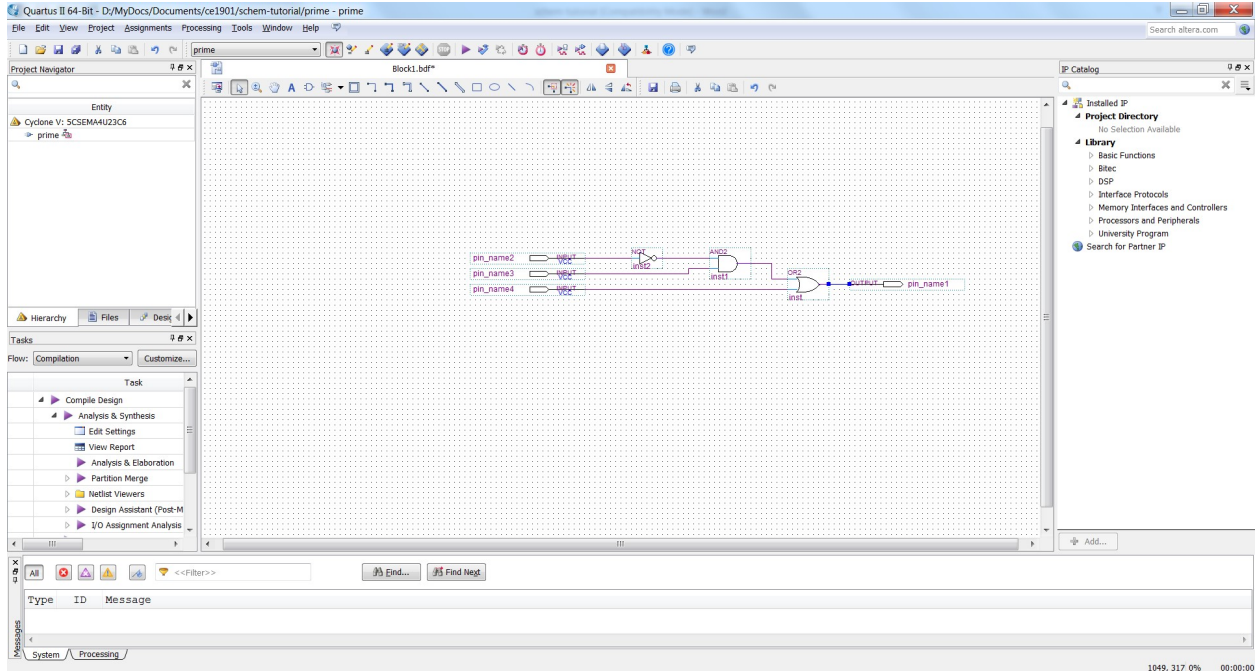

Corners can be made by clicking as you drag the mouse.

Drawing blueprints is fundamental in engineering. It's sort of an art form! Your blueprint doesn't have to look exactly like the one shown. Your signal wires might bend earlier or remain straight for that matter. But, the signal wires and gates must be connected together as shown in order to guarantee that electricity flows correctly for the design problem.

Your instructors will evaluate your drawings during the quarter for "visual noise." In other words, try to eliminate unnecessary right angles, the number of wires that cross in a diagram, and keep things like the inputs lined up to create a nice "visual line."

16. **Name** the inputs and outputs by **double-clicking** each one and typing its name. In this diagram, the inputs are names A, B, and C from top to bottom. The single output is named PRIME.
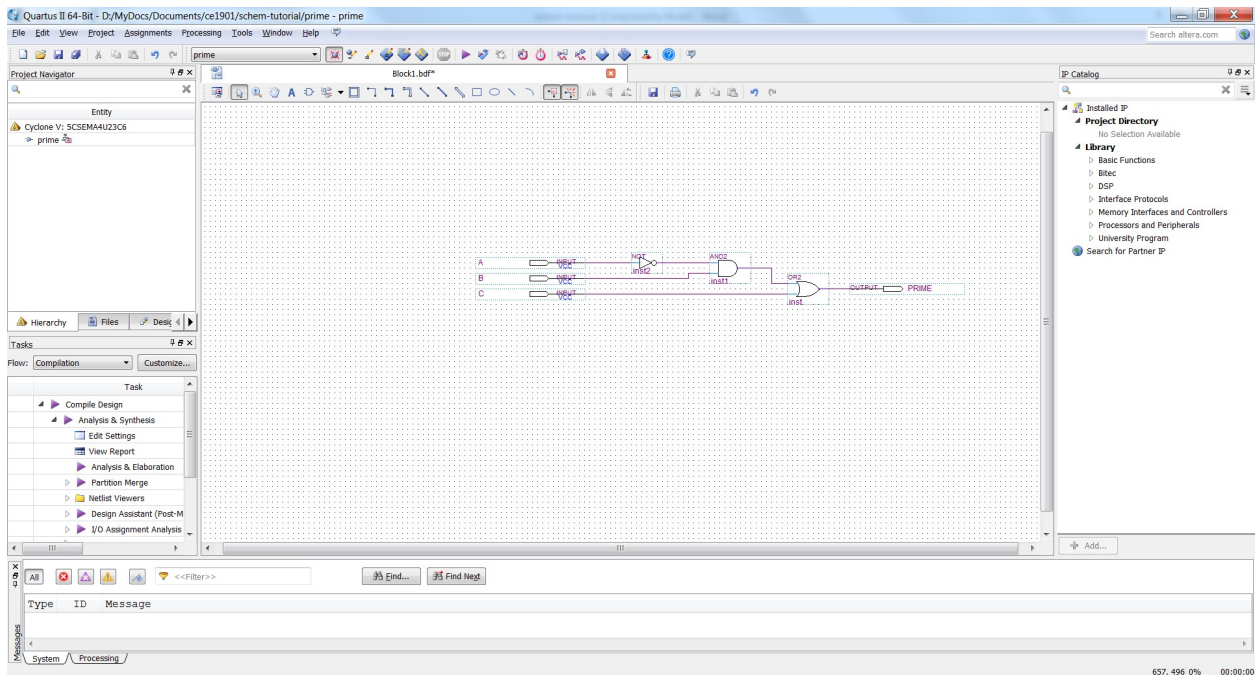
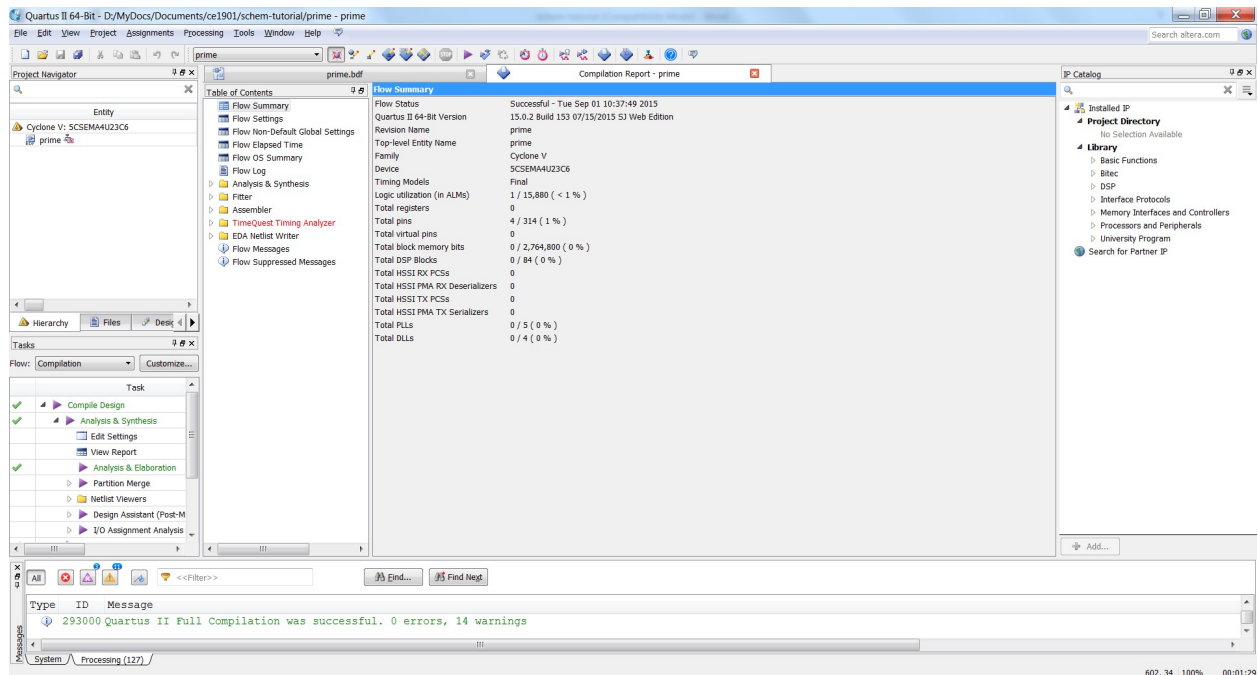17. **Save** the completed schematic.

Use CTRL-S or the "Save" icon. Note that Quartus will present a "Save As" dialog box in the project folder with a pre-assigned name of "prime". Just select the "Save" button.

18.   **Compile** the design to check for errors in wire interconnection. **Choose** "Start Compilation" from the "Processing" menu or just click the compile diamond (arrow) just to the right of the gray stop sign icon.
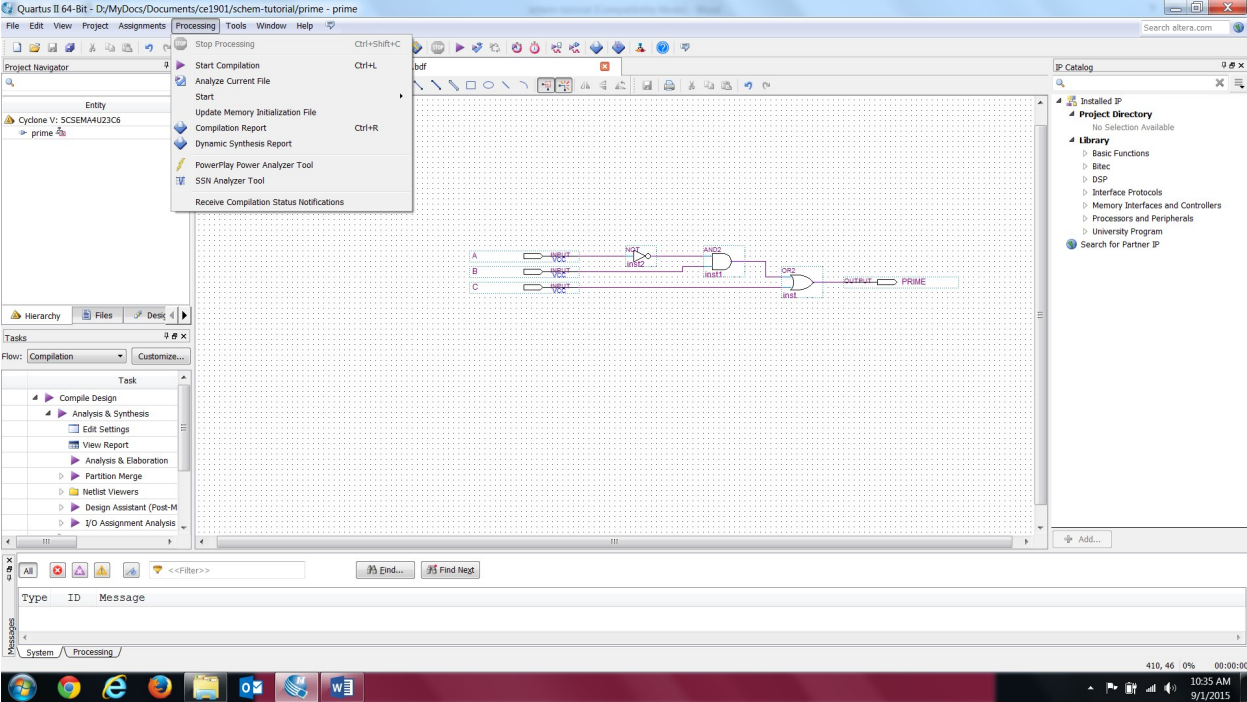
Lots of activity occurs during compilation. Quartus is verifying wire connections, creating a mapping of technologies used in the design, fitting the technology mapping to an automatically chosen integrated circuit chip, creating a programming file for that chip, etc. This process is known as "silicon compilation" or "compile-place-route" in modern digital logic design environments. Keep reading the tutorial to see how you should use the message windows to verify your work.

19. **Wait** patiently while Quartus compiles the design and then **verify** that the compile completed successfully.
    A. **Carefully** check wiring and names if the compiler found errors.
    B. **Recompile** until you achieve successful compilation.
    C. **Note** that successful compilation results in a **Flow Status**: Successful.
    D. **Note** that the "device" should match 10M50DAF484C7G. Select the correct chip using menu choice Assignments:Device if it doesn't match **because** the correct chip wasn't chosen from the New Project Wizard during project creation.
   E. **Note** that compilation is much faster if the computer is plugged into AC power.

20. **Close** the compilation report tab by clicking the tab close box (small X) on the tab.

This finishes the basic steps to drop components into a schematic, wire the components together, name inputs and outputs, and complete the compilation of the project to verify connectivity. The next part of the tutorial will explore simulating the circuit to verify correct operation.

21.   **Choose** the University Program verification waveform file (VWF) from the
   File:New dialog box. The simulation waveform editor will open.
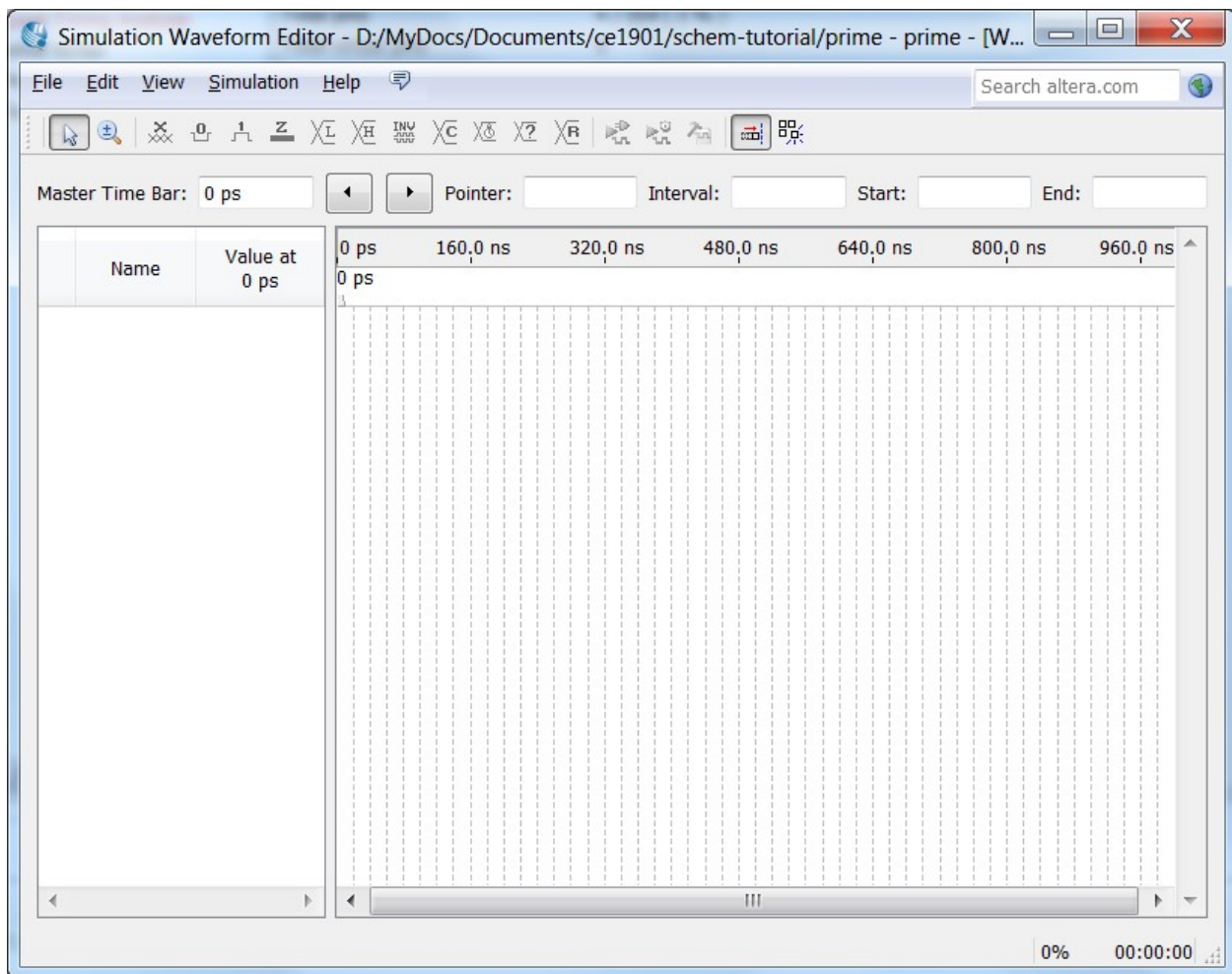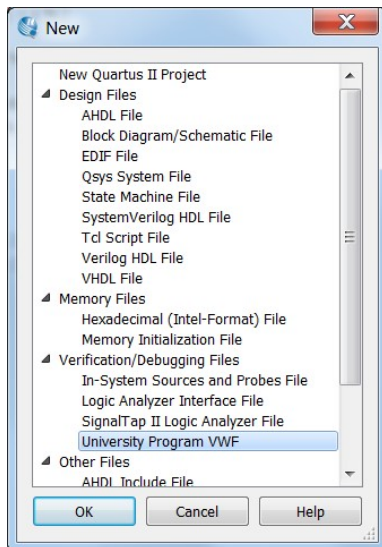
22. Right-click under the "Name" column. Choose "Insert Node or Bus..." from the "Insert" submenu.
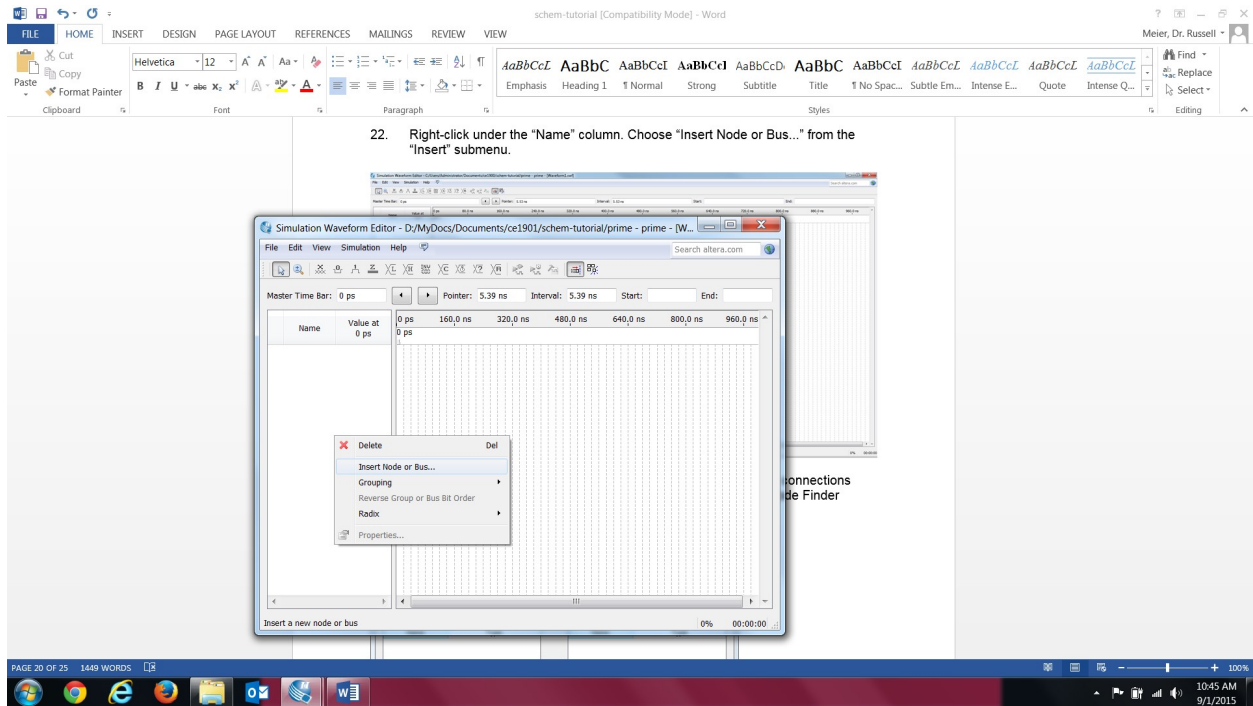
23. **Click** the "Node Finder..." button. Quartus calls all pins and gate connections nodes. Thus, all electrical signals are nodes in the circuit. The Node Finder Dialog box will open.
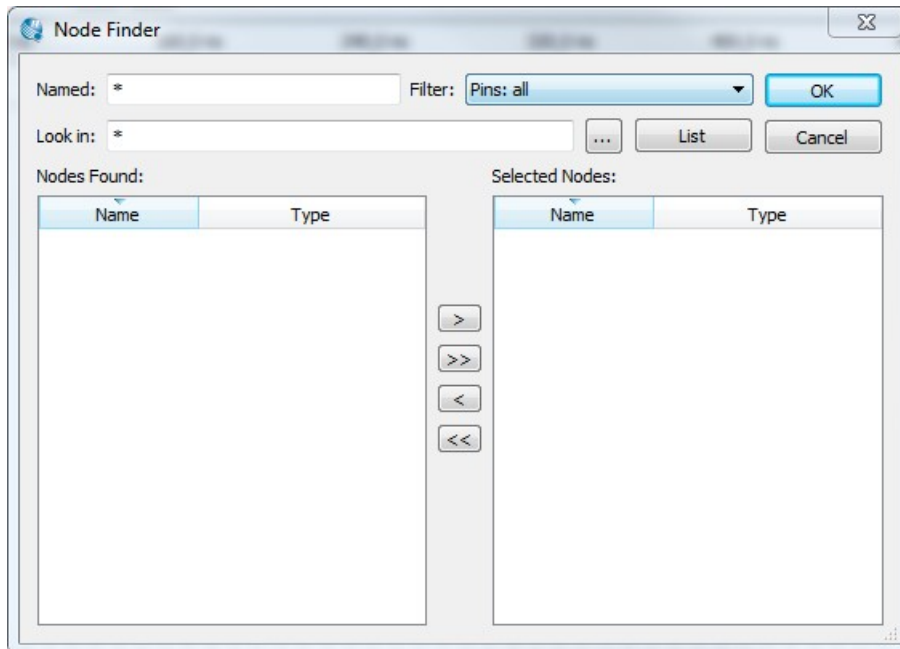
24. **Select** signals for viewing on the electrical simulation.
    A. **Click** the List button.
    B. **Highlight** all the pins in the left panel and copy them to the right panel –
       the "selected nodes" panel – by using the copy button ">". This chooses all
       the pins as signals of interest for the simulation.
    C. **Click** the OK button to close the dialog box.
    D. **Click** the OK button to close the second dialog box.
    E. **Note** that the waveform workspace panel will now show the circuit
       signals with no energy on them. Signal PRIME is shown with
       "unknown" voltage because it is an output and the simulation has not yet
   been executed.
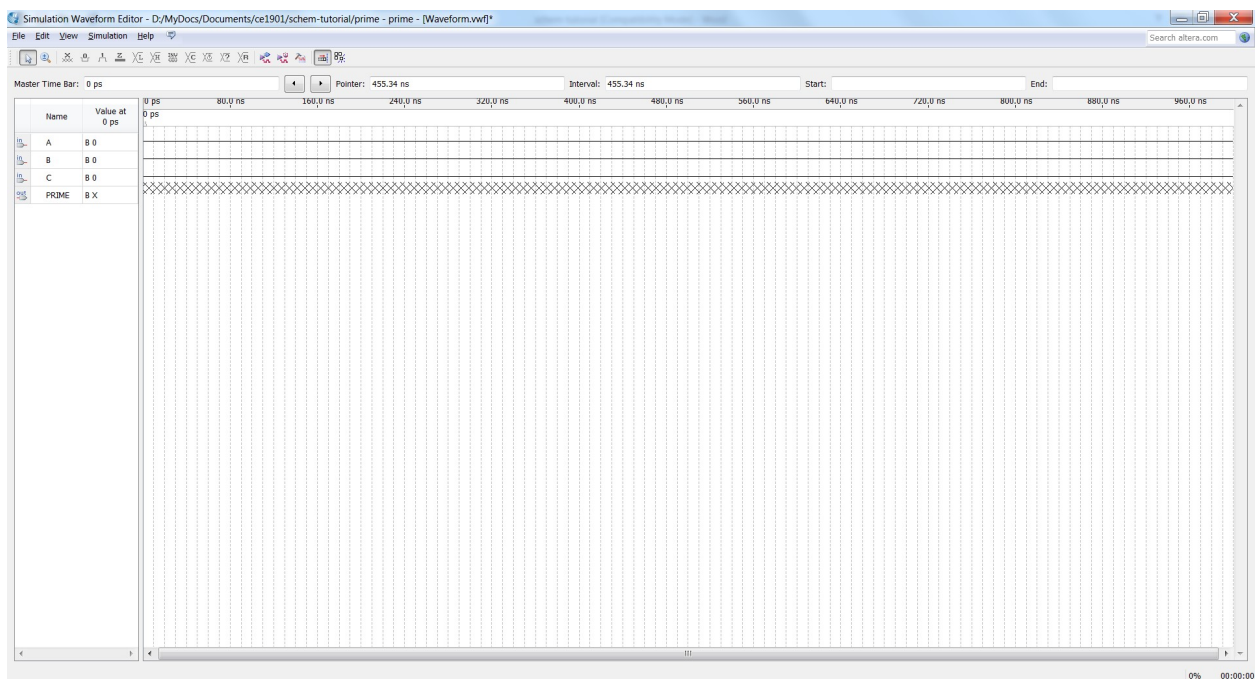
The "Name" sub-panel can be "pulled" to the right using the mouse so
that the entire "prime" signal name can be read.

25. **Group** the input bits into a 3-bit binary number.
   A. **Arrange** the signals so that A is at the top of the inputs, B follows, and C is the last input bit. The signals may already be correctly ordered.
   B. **Highlight** signals A, B, and C using the Shift Key and mouse clicks.
   C. **Right-click** on the signal set.
   D. **Choose** Group from the Grouping submenu.
   E. **Note** that grouping allows you to write binary numbers onto the signal group. This is just like signals sitting side-by-side in a truth table.
   F. **Name** the group ABC when asked. Because A is the top signal, it is the most-significant bit and C is the least-significant bit in the group.
   G. **Set** the radix to Unsigned Decimal.
   H. **Click** Ok to close the group dialog box.
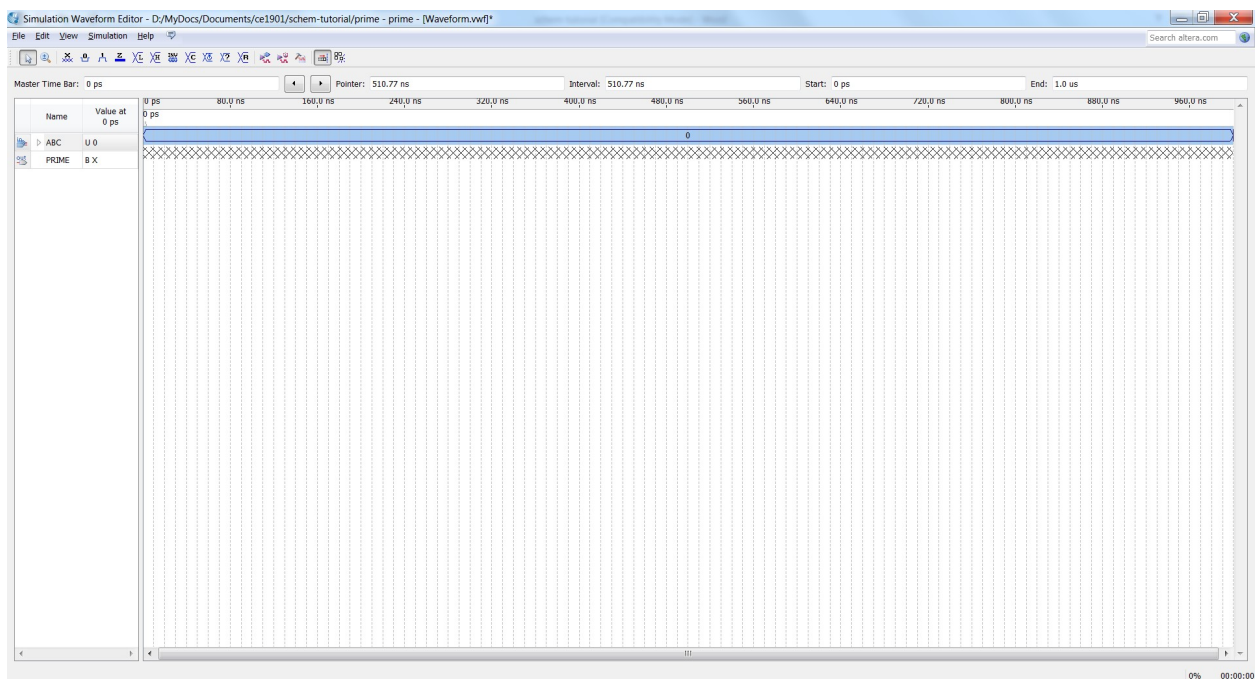
26. **Overwrite** a counting sequence onto the ABC signal group.
   A. **Highlight** the ABC group by clicking its name in the name column.
   B. **Choose** the counting sequence icon from the tool bar. It has a C on it!
   C. **Note** that the simulation window shows 1000 nanoseconds of time. Three binary input signals encode the numbers 0 through 7 for a total of eight possible numbers. Good simulation practice would examine the PRIMEcresult for each of these possible inputs exactly once. Thus, 1000 ns divided by 8 possible input patterns gives 125 ns of time per input pattern.
   D. **Set** the Count Every entry box to 125 ns. **Read item c** above for an explanation of this number.
   E. **Click** the OK button.
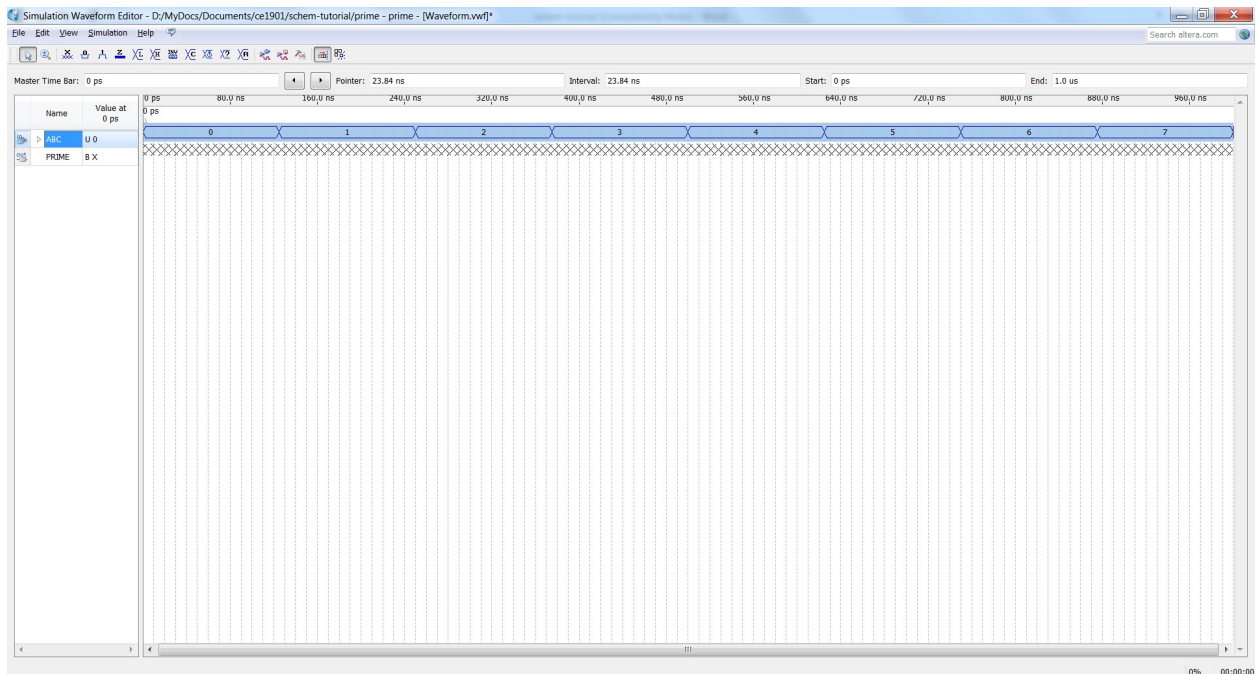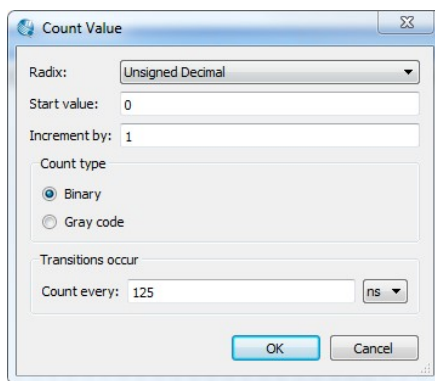
27.   **Choose** Run Functional Simulation from the Simulation Menu.
   A.   **Accept** the default waveform filename.
   B.   **Significant** work will appear on your screen as Quartus simulates.
   C.   **View** the simulation results! Decimal 1, 2, 3, 5, and 7 are prime and thus the gate circuit drives energy onto the PRIME signal for only those values.
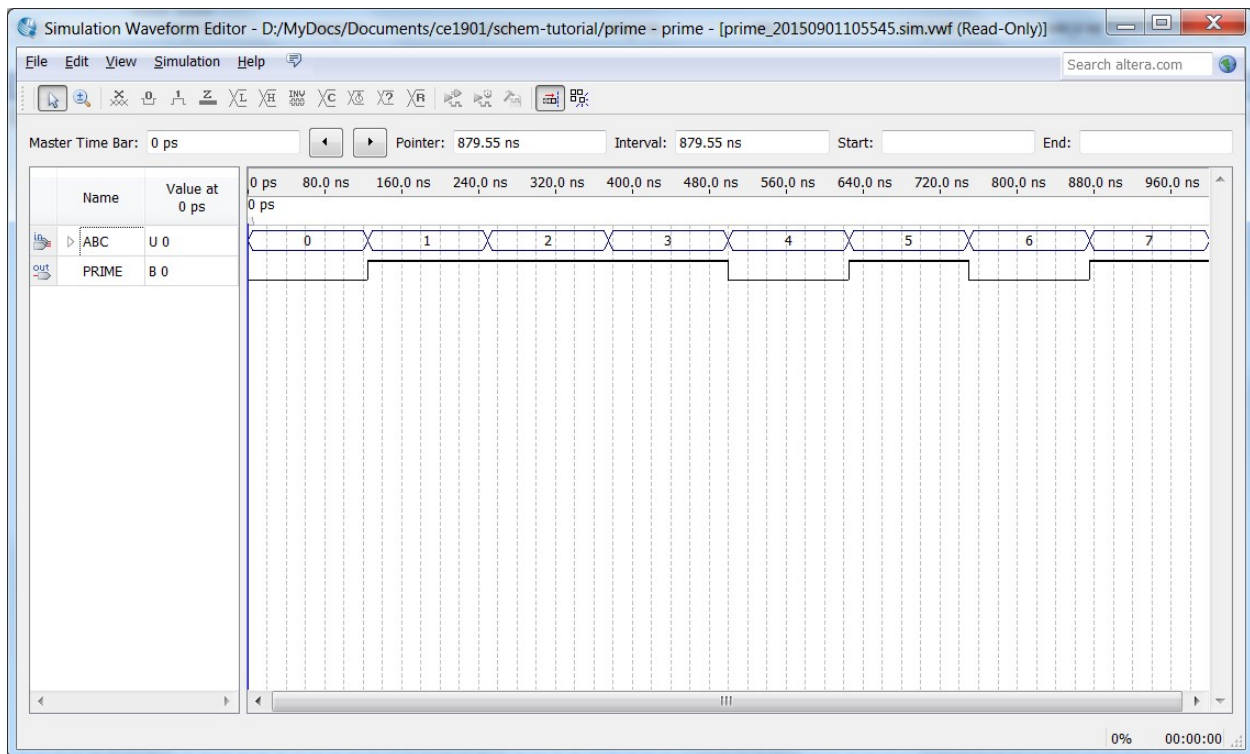
28.   **Close** the simulator by **clicking** the close (X) icons in the simulator waveform editor and results windows.

29.   **Close** the Quartus project by **choosing** Close Project from the Quartus File menu.

This concludes the Quartus schematic and simulation tutorial. **Quit** Quartus using by **choosing** Exit from the File menu.