CE1911 BASIC STATIC MEMORY REVIEW SHEET

Memory is the ability to retain information indefinitely. In humans, memory retains patterns experienced by our bodies through its sensors. These memories include reflexive responses learned from past experiences such as touching hot surfaces, as well as behaviors and information learned by repetition. Human memory is a complex system of cell interconnections controlled by neurotransmitters. Reinforcement of stored information strengthens the biological memory of it.

Computer memory retains voltage patterns representing binary numbers. Computer programmers and computer architects attach meaning to these numbers and use them to direct calculation and computer behavior. For example, a computer program written in C or Swift is a sequence of control and calculation steps that occur through time. This sequence is converted to binary numbers stored in program memory. The computer executes each instruction by reading it from program memory, deciphering it into control signals for the functional logic elements of the calculation engine, and storing any resulting data value from the instruction back to memory. As another example, the frame buffer memory is a memory that contains all pixel data currently displayed on the screen. Each light pixel has red intensity, green intensity, and blue intensity encoded as binary numbers and these numbers are stored in the frame buffer. The display hardware reads these pixel RGB numbers and uses them to control the color of light emitted from each pixel of the display.

Computer architects have developed different types of computer memories. Each type works to optimize one or more of these areas: speed, size, power, and cost.

Static memory does not lose its voltages as long as the systems supplies battery power to the memory circuit. This adjective "static" describes this stability in memory. Retention of the data through time occurs because the output of the memory feeds back to become its input again. This constantly reinforces the retained value and makes a stable memory. The reinforcement circuit requires multiple gates and thus multiple transistors. Because this type of memory does not forget, it does not need to be periodically refreshed to ensure data integrity. This optimizes speed because the system does not need to take any units of time to refresh forgotten data.
[**Advantage: speed**] [**Disadvantage: size, cost-per-bit**]

Dynamic memory, on the other hand, optimizes size and thus provides larger memory circuits. Multiple gates do not provide reinforcement of the remembered value. Instead, this type of memory stores logic-1 as electrical charge on a single capacitor. The capacitor immediately begins decaying the stored voltage toward logic-0 because of parasitic resistive-capacitive effects caused in built material. The RC time constant determines the decay rate. Electric circuit theory courses will cover the principles of RC time constants and capacitive decay. This type of memory forgets stored logic-1s because the capacitor parasitically decays logic-1 to logic-0! Thus, a refresh controller must periodically refresh every bit of memory. This controller is another piece of hardware that reads each memory bit and rewrites it. The controller must move through all the memory bits before any bit forgets its stored logic-1. Thus, there is an operational speed disadvantage. A computer program attempting to access memory may have to wait for the refresh controller to finish working on the current set of bits before the memory system grants access to store data into memory.
[**Advantage: size, cost-per-bit**][**Disadvantage: speed**]

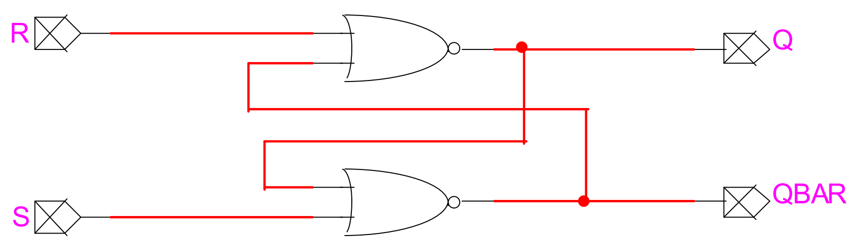
CE1911 explores static memory circuits while CE3101 introduces dynamic memory circuits.

STATIC MEMORY COMPONENT SUMMARY

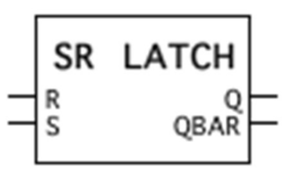
- The basic memory element stores one data of bit.
- One-bit memories come in two types: latches and flip-flops.
- Latches are transparent to input changes when enabled.
- Flip-flops use a clock edge to take an instant snapshot of the input voltage.
- Engineers more commonly use flip-flops because the snapshot behavior allows arithmetic circuits to use the entire clock period to calculate the next number that will be stored into memory.
- A register is an n-bit wide memory that stores a single n-bit wide number. Build a register by connecting n flip-flops to their corresponding input (D0, D1, etc.) with a shared clock and a shared reset.

CIRCUIT DIAGRAMS

SR LATCH



SR LATCH SYSTEM-LEVEL SYMBOL

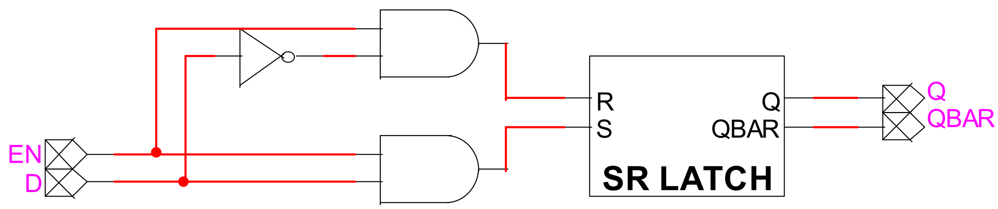


TRUTH TABLE

S	R		Q	BEHAVIOR
0	0		Q0	HOLD
0	1		0	RESET
1	0		1	SET
1	1		X	Not Allowed

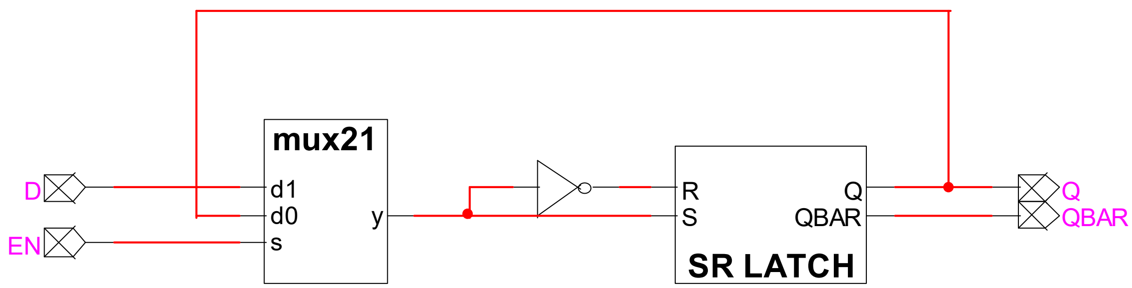
[Disadvantage: The circuit does not correctly produce Q and QBAR if both inputs are active.]

D LATCH BUILT USING GATES



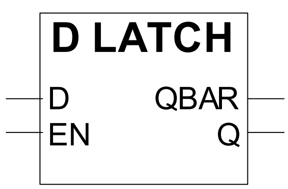
FIXES THE FOUNDATIONAL FLAW IN SR LATCH.
GATES PREVENT R AND S FROM BOTH BEING 1 AT THE SAME TIME

D LATCH BUILT USING A MULTIPLEXER



FIXES THE FOUNDATIONAL FLAW IN THE SR LATCH.
INVERTER PREVENTS R AND S FROM BOTH BEING 1 AT THE SAME TIME

D LATCH SYSTEM-LEVEL SYMBOL



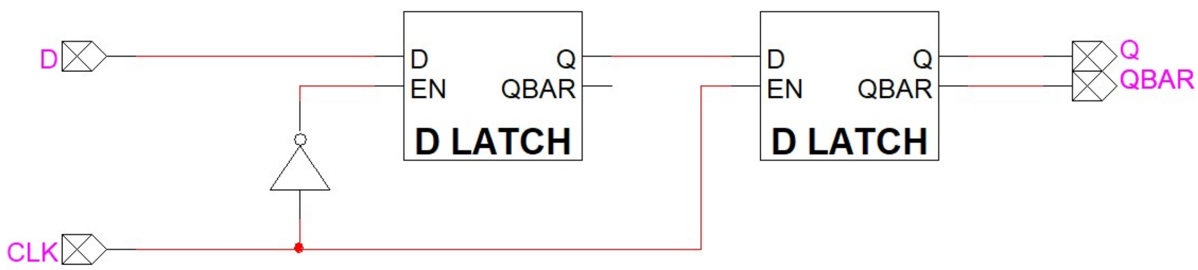
TRUTH TABLE

EN	D		Q	BEHAVIOR
0	0		Q_0	HOLD
0	1		Q_0	HOLD
1	0		0	STORE 0 (RESET)
1	1		1	STORE 1 (SET)

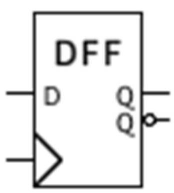
[Advantage: All control inputs cause appropriate memory behavior.]

LATCHES ARE TRANSPARENT. FLIP FLOPS TAKE A SNAPSHOT OF VOLTAGE AT THE CLOCK EDGE

RISING-EDGE TRIGGERED D FLIP FLOP



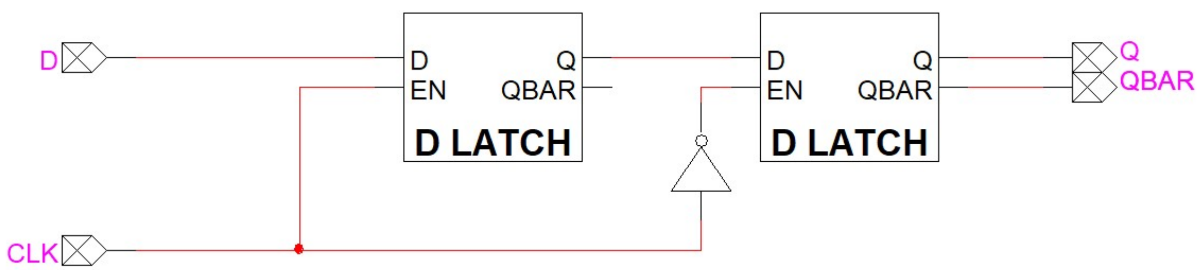
D FLIP FLOP SYSTEM-LEVEL SYMBOL



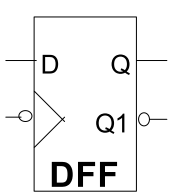
TRUTH TABLE

D	CLK		Q	BEHAVIOR
0	↑		0	SNAP SHOT SAMPLE
1	↑		1	SNAP SHOT SAMPLE
X	1		Q_0	HOLD
X	0		Q_0	HOLD

FALLING-EDGE TRIGGERED D FLIP FLOP



D FLIP FLOP SYSTEM-LEVEL SYMBOL

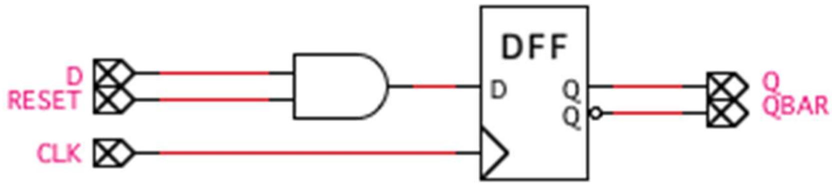


TRUTH TABLE

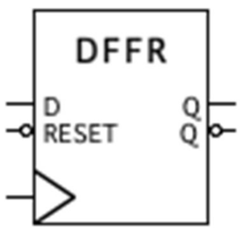
D	CLK		Q	BEHAVIOR
0	↓		0	SNAP SHOT SAMPLE
1	↓		1	SNAP SHOT SAMPLE
X	0		Q_0	HOLD
X	1		Q_0	HOLD

[Advantage: snapshot behavior allows computation circuits to fully use clock period]

D FLIP FLOP WITH SYNCHRONOUS RESET



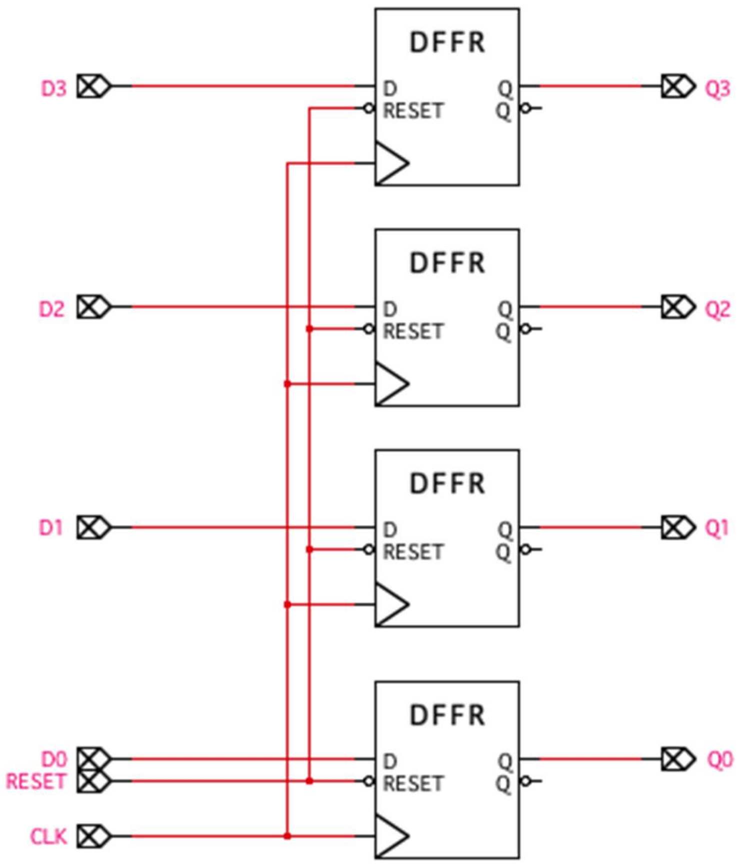
D FLIP FLOP SYSTEM-LEVEL SYMBOLS



TRUTH TABLE

D	CLK	RESET	Q	BEHAVIOR
0	↑	1	0	SNAP SHOT SAMPLE
1	↑	1	1	SNAP SHOT SAMPLE
X	↑	0	0	SYNCH RESET
X	1	X	Q0	HOLD
X	0	X	Q0	HOLD

4-BIT REGISTER BUILT FROM DFFR COMPONENTS



D FLIP FLOP SYSTEM-LEVEL SYMBOLS