NAME: _____

ITEM	DEMO ON TIME	GRADING POINTS
SAT-UPDWN3 state diagram, truth table, and equation derivation		____ / 2
SAT-UPDWN3 schematic and RTL		____ / 2
SAT-UPDWN3 simulation waveforms		____ / 2
EVENODD3 state diagram, truth table, and equation derivation		____ / 2
EVENODD3 schematic and RTL		____ / 2
EVENODD3: Quartus simulation showing rst, up, and down behaviors		____ / 2
SAT-EVENODD3: state machine diagram		____ / 2
SAT-EVENODD3: equation derivations		____ / 2
SAT-EVENODD3: Quartus simulation showing rst, up, and down behavior.		____ / 2
Completed by the due date.		____ / 2
TOTAL		___ / 20 = _____ % ____ / 10

- **Print** this coversheet and attach it to the top of your **laboratory submission packet**.
- **Packets** must always include:
  - **Design files**: blueprints, VHDL, synthesis generates RTL diagrams
  - **Test files**: simulation waveforms, oscope photos, and photos of any built circuits.
- **Submit by**: 5:00 p.m. one academic day after your laboratory period.
  One academic day after Friday is Monday.
- **How to submit (choose one):**
  - **Pin** to Dr. Meier's office bulletin board (L-349).
  - **Slide** under Dr. Meier's office door (L-349).
  - **Hand** to Dr. Meier if he is in his office (L-349).
  - **Put** in Dr. Meier's mailbox (L-350).