NAME: _____

ITEM	DEMO ON TIME	GRADING POINTS
State machine design: next state logic, output logic		____ / 3
VHDL source code quality: commented, indented, visual line, etc.		____ / 2
Quartus simulation showing reset and operational behavior.		____ / 2
Laboratory demonstration and documentation packet quality		____ / 3
TOTAL		___ / 10 = _____ %

- **Print** this coversheet and attach it to the top of your **laboratory submission packet**.
- **Packets** must always include:
  - **Design files**: blueprints, VHDL, synthesis generates RTL diagrams
  - **Test files**: simulation waveforms, oscope photos, and photos of any built circuits.
- **Submit by**: 5:00 p.m. one academic day after your laboratory period.
  One academic day after Friday is Monday.
- **How to submit (choose one):**
  - **Pin** to Dr. Meier's office bulletin board (L-349).
  - **Slide** under Dr. Meier's office door (L-349).
  - **Hand** to Dr. Meier if he is in his office (L-349).
  - **Put** in Dr. Meier's mailbox (L-350).