CE1911 LABORATORY
SYSTEM DESIGN SPECIFICATIONS

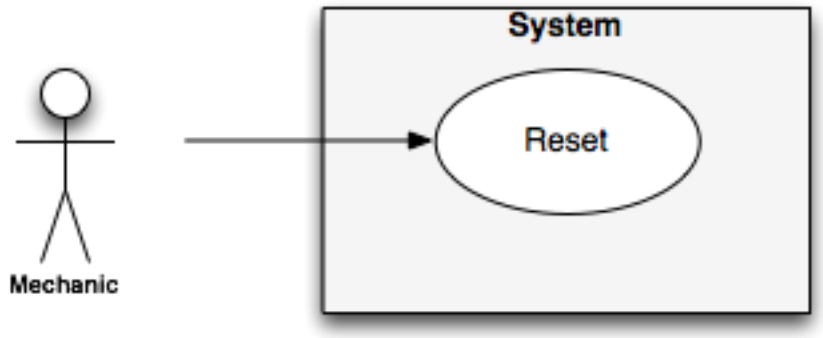
DESCRIPTION

This specification describes and defines the basic requirements of the CE1911 electronic fuel ignition system. The system generates digital pulses on four output signals. Each output signal controls the spark mechanism of one spark plug in a four-cylinder automobile engine. Each output pulse causes the corresponding spark plug to ignite the vaporized fuel mixture in the cylinder. The ignition of fuel causes gas expansion that pushes the piston away from the spark plug thus creating the power stroke that rotates the crankshaft of the engine. The crankshaft motion transfers to the gear train and eventually the axels of the vehicle.

REQUIREMENTS

1. The system must generate periodic pulse waveforms on four output signals.
2. The system must respond to a reset signal activated by an automotive mechanic.
3. The system must operate from 12V automotive power or USB supplied power.
4. The system must operate in a high vibration environment.
5. The system must operate in a high temperature environment.

USE-CASE DIAGRAM



USE CASE EVENTS

1. Reset Event

    A. The automotive mechanic resets the system.
    B. The system identifies the reset request.
    C. The system responds by driving all spark output to logic 0.

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SPECIFICATION OF SYSTEM INPUTS AND OUTPUTS

1. System Inputs

   A. The system provides a digital pushbutton to request the system clear the memory register.

      i. The pushbutton produces logic 0 or logic 1.
      ii. The pushbutton reset request is **active when low** (logic-0).
      iii. The pushbutton reset request **synchronizes** to the rising-edge of the clock.
      iv. The name of the pushbutton signal is **RST**.

2. System Outputs

   A. The system creates four digital outputs called Y3, Y2, Y1, and Y0.

      i. Output Y3 connects to the spark mechanism of cylinder 3.
      ii. Output Y2 connects to the spark mechanism of cylinder 2.
      iii. Output Y1 connects to the spark mechanism of cylinder 1.
      iv. Output Y0 connects to the spark mechanism of cylinder 0.
      v. A spark fires as the output transitions from logic 0 to logic 1.

FUNCTIONAL SPECIFICATION

The system is a Moore finite state machine.

1. The machine enters the reset state when the active-low pushbutton is pushed.
2. The machine stays in the reset state if the pushbutton is pushed.
3. The machine uses twenty states to generate the repeating pulse train shown in Figure 1.
4. The total number of machine states is twenty-one: reset and twenty waveform generation states.
5. The reset state has all outputs Y3, Y2, Y1, and Y0 equal to 0.
6. The waveform generation states have at least one output equal to 1.

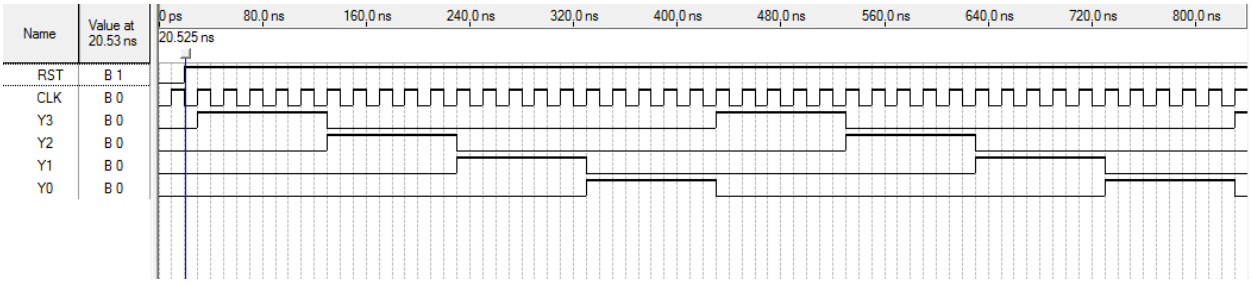

Figure 1: Electronic Fuel Ignition Operational Timing Diagram with Reset Event

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MOORE MACHINE MODEL

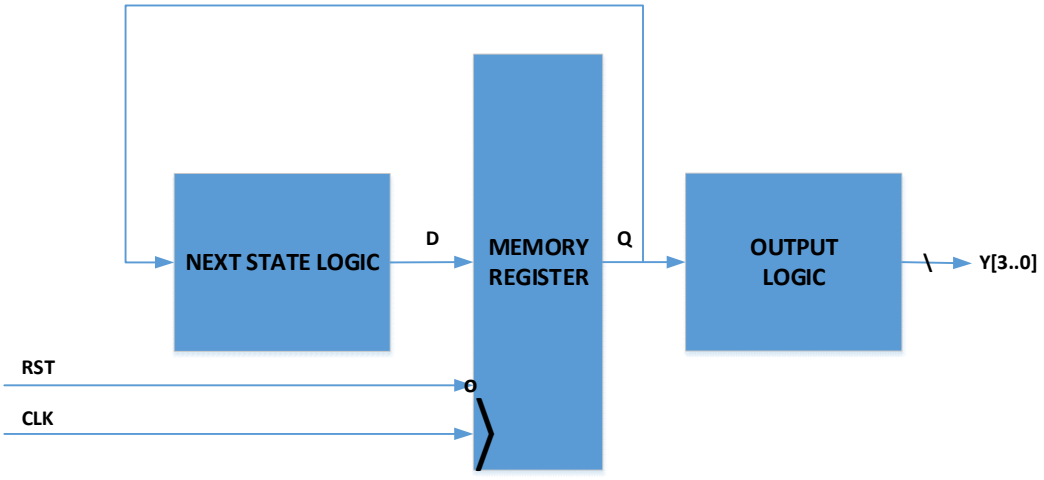

Figure 2: Next State Logic Advances Stored State and Output Logic Generates Pulse Train

IMPLEMENTATION TECHNOLOGY

1. A single behavioral VHDL file describes the complete system.
2. The system resides as a configured circuit in an off-the-shelf Altera DE10-Lite board.
3. Table 1 documents expected project files.
4. Table 2 documents Altera DE10-Lite pin assignments.

Table 1: Project Files

PROJECT NAME: ENGINE			
FILENAME	**FORMAT**	**NEW OR REUSE**	**CIRCUIT**
engine.vhd	behavioral VHDL	new	complete Moore machine implementation

Table 2: DE10-Lite Pin Assignments

SIGNAL NAME	I/O	DE10 PIN	DE10-LITE I/O DEVICE	REFERENCE IN DE10-LITE USER MANUAL
CLK	input	P11	clock circuit	Page 25
RST	input	B8	pushbutton key 0	Page 26
Y[3]	output	W9	GPIO header pin GPIO[3]	Page 31
Y[2]	output	V9	GPIO header pin GPIO[2]	Page 31
Y[1]	output	W10	GPIO header pin GPIO[1]	Page 31
Y[0]	output	V10	GPIO header pin GPIO[0]	Page 31

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SIMULATION TEST BENCH

A VHDL test bench verifies the Figure 1 reset and operational use cases.

1. Review testbenches from previous labs for examples of testbench syntax.
2. Write a clock process that generates a 20 ns clock period.
3. Write a tester process that drives RST active low for two clock periods.
4. Ensure that RST does not rise at the same time as a rising clock edge.
5. Ensure that the test process ends with an infinite **wait;** statement.
6. Simulation end-time matches Figure 1.
7. ModelSim-Altera test bench simulation verifies operation.

LABORATORY TESTING

Laboratory testing verifies the Figure 1 reset and operational use cases.

1. Use a USB Analog Discovery kit or a laboratory logic analyzer to verify the electric signals.
2. Connect outputs Y3 through Y0 to a USB Analog Discovery kit or a laboratory logic analyzer.
3. Connect the logic analyzer ground to a ground pin on the DE10-Lite GPIO header.
4. Verify that pulses are present.
5. Measure the clock period and verify that it is 20 ns.
6. Measure the width of each output pulse and verify that each is 100 ns.

HINTS

1. The timing diagram shows a repeating pattern of waveforms.
2. The timing diagram shows a 20 ns sample clock period (50MHz).
3. Each output waveform stays high for five states for a total of 100 ns.
4. There are twenty total states to generate the pulse train and one reset state.
5. The machine resets into the reset state called S0 and transitions to state S1 from reset.
6. Y3 is high in S1, S2, S3, S4, and S5.
7. Other outputs are high in other states.