CE1911 LABORATORY
SYSTEM DESIGN SPECIFICATIONS

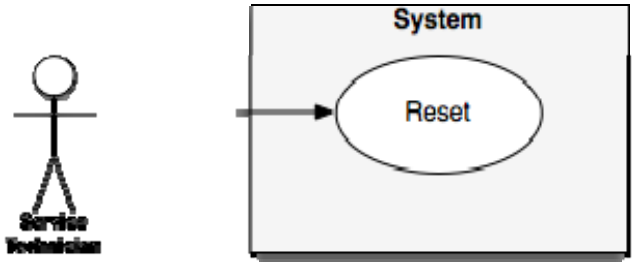
DESCRIPTION

This specification describes and defines the basic requirements of the CE1911 traffic light controller. The controller coordinates traffic flow at a standard **+** shaped intersection without turn lanes by generating six digital voltages that turn on and off the red, yellow, and green lights. The controller does not coordinate pedestrian flow because this intersection is in a rural area with no sidewalks.

REQUIREMENTS

1. The system must never allow traffic to move simultaneously in both directions.
2. The system must reset into a state with traffic stopped in both directions.
3. The system must provide 20 seconds of green light.
4. The system must provide 6 seconds of yellow light.
5. The system must provide 3 seconds of red light in both directions before green.
6. The system must provide status information on a 7-segment display.
7. The system must operate from standard line power or USB supplied power.

USE-CASE DIAGRAM



USE-CASE EVENTS

1. Reset Event

    A. The service technician or a power-on event resets the system.
    B. The system identifies the reset request.
    C. The system responds by lighting red lights in both traffic directions.

CE1911 LABORATORY
SYSTEM DESIGN SPECIFICATIONS

SPECIFICATION OF SYSTEM INPUTS AND OUTPUTS

1. System Inputs

   A. The system provides a digital pushbutton to request system reset.

      i. The pushbutton produces logic 0 or logic 1.
      ii. The pushbutton reset request is **active when low** (logic-0).
      iii. The pushbutton reset request **synchronizes** to the rising-edge of the clock.
      iv. The name of the pushbutton signal is **RST.**

2. System Outputs

   A. The system creates four digital outputs called R1, Y1, G1, R2, Y2, G2.

      i. Output R1 connects to the red LED lamps mounted on the poles facing direction one.
      ii. Output Y1 connects to the yellow LED lamps mounted on the poles facing direction one.
      iii. Output G1 connects to the green LED lamps mounted on the poles facing direction one.
      iv. Output R2 connects to the red LED lamps mounted on the poles facing direction two.
      v. Output Y2 connects to the yellow LED lamps mounted on the poles facing direction two.
      vi. Output G2 connects to the green LED lamps mounted on the poles facing direction two.
      vii. The outputs are grouped in the order R1, Y1, G1, R2, Y2, G2 as an output bus LEDS[5..0].

   B. The system provides fourteen digital output signals that drive the LED segments of a two character 7-segment display mounted in the system pedestal located on the street corner. A service technician can monitor system behavior by reading status text.

      i. The system generates status text G 1, YL, YE, G2 on a 14-bit output bus.
      ii. The G 1 status text represents traffic moving in direction 1. (GO 1)
      iii. The YL status text represents yellow lights slowing traffic.
      iv. The YE status text represents traffic stopped in both directions.
      v. The G2 status text represents traffic moving in direction 2.

FUNCTIONAL SPECIFICATION

The system is a Moore finite state machine.

1. The machine enters the reset state when the active-low pushbutton is pushed.
2. The reset state has traffic stopped in both directions.
3. The machine coordinates traffic flow and status outputs using its output signals. Figure 1 documents the lamp control signals in top-to-bottom order R1, Y1, G1, R2, Y2, G2.

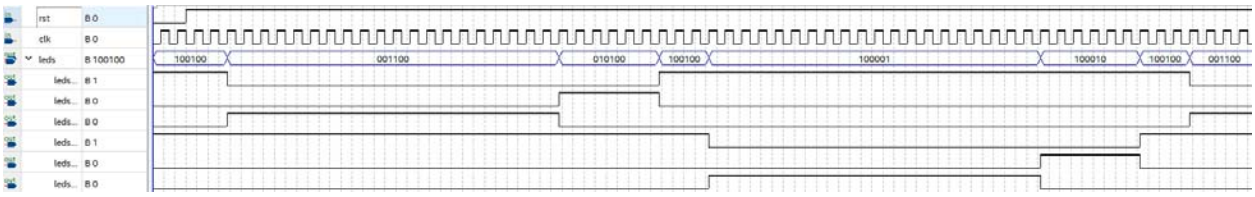


Figure 1: Traffic Light Controller with Reset Event

CE1911 LABORATORY
SYSTEM DESIGN SPECIFICATIONS

MOORE MACHINE MODEL

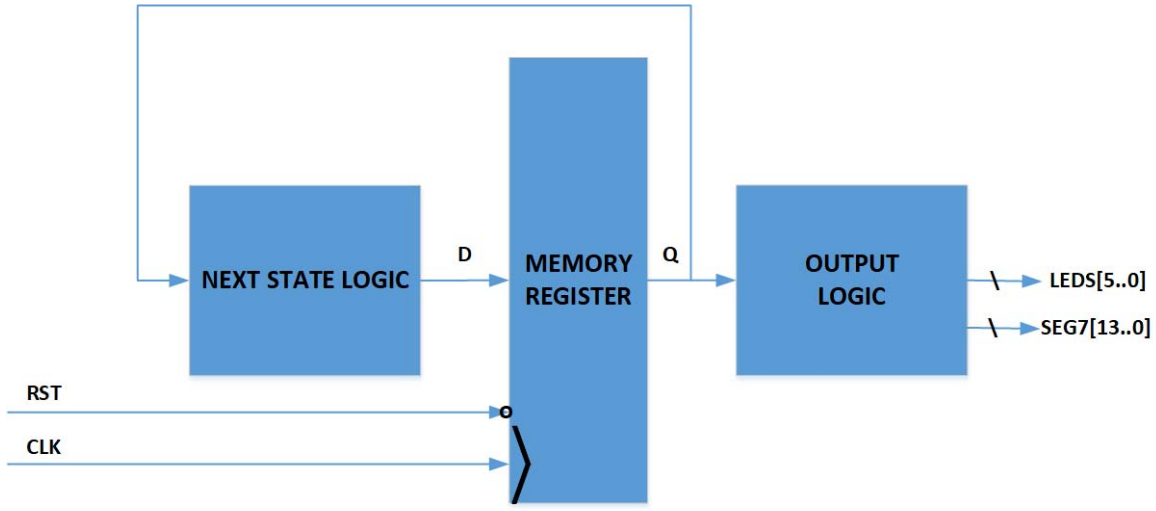


Figure 2: Next State Logic Advances Stored State and Output Logic Generates LED Signals and Status Text

IMPLEMENTATION TECHNOLOGY

1. A single behavioral VHDL file describes the complete system. The use of **type states** is required.
2. The system resides as a configured circuit in an off-the-shelf Altera DE10-Lite board.
3. Table 1 documents expected project files.
4. Tables 2 and 3 documents Altera DE10-Lite pin assignments.

Table 1: Project Files

PROJECT NAME: ENGINE			
FILENAME	**FORMAT**	**NEW OR REUSE**	**CIRCUIT**
traffic.vhd	behavioral VHDL	new	complete Moore machine implementation

Table 2: DE10-Lite Pin Assignments for System Inputs and Lamp LED Outputs

SIGNAL NAME	I/O	DE10 PIN	DE10-LITE I/O DEVICE	REFERENCE IN DE10-LITE USER MANUAL
CLK	input	P11	clock circuit	Page 25
RST	input	B8	pushbutton key 0	Page 26
LEDS[5] (R1)	output	J20	HEX5 segment 0	Pages 29 and 30
LEDS[4] (Y1)	output	N20	HEX5 segment 6	Pages 29 and 30
LEDS[3] (G1)	output	N18	HEX5 segment 3	Pages 29 and 30
LEDS[2] (R2)	output	F21	HEX3 segment 0	Pages 29 and 30
LEDS[1] (Y1)	output	E17	HEX3 segment 6	Pages 29 and 30
LEDS[0] (G2)	output	C19	HEX3 segment 3	Pages 29 and 30

Table 3: DE10-Lite Pin Assignments for Status Text Outputs

SIGNAL NAME	I/O	DE10 PIN	DE10-LITE I/O DEVICE	REFERENCE IN DE10-LITE USER MANUAL
SEG7[13]	output	C18	HEX1 segment 0	Pages 29 and 30
SEG7[12]	output	D18	HEX1 segment 1	Pages 29 and 30
SEG7[11]	output	E18	HEX1 segment 2	Pages 29 and 30
SEG7[10]	output	B13	HEX1 segment 3	Pages 29 and 30
SEG7[9]	output	A17	HEX1 segment 4	Pages 29 and 30
SEG7[8]	output	A18	HEX1 segment 5	Pages 29 and 30
SEG7[7]	output	B17	HEX1 segment 6	Pages 29 and 30
SEG7[6]	output	C14	HEX0 segment 0	Pages 29 and 30
SEG7[5]	output	E15	HEX0 segment 1	Pages 29 and 30
SEG7[4]	output	C15	HEX0 segment 2	Pages 29 and 30
SEG7[3]	output	C16	HEX0 segment 3	Pages 29 and 30
SEG7[2]	output	E16	HEX0 segment 4	Pages 29 and 30
SEG7[1]	output	D17	HEX0 segment 5	Pages 29 and 30
SEG7[0]	output	C17	HEX0 segment 6	Pages 29 and 30

SIMULATION TEST BENCH

A VHDL test bench verifies the Figure 1 reset and operational use cases.

1. Write a clock process that generates a 1000 ms clock period.
2. Write a tester process that drives RST active low for two clock periods.
3. Ensure that RST does not rise at the same time as a rising clock edge.
4. Ensure that the test process ends with an infinite **wait;** statement.
5. Calculate simulation end-time so that it matches the number of clock periods shown in Figure 1.
6. ModelSim-Altera test bench simulation verifies operation.

LABORATORY TEST PLAN

Laboratory testing verifies the Figure 1 reset and operational use cases.

1. Add the clock divider shown in Figure 3 to the **traffic.vhd** file. The divider slows the DE10-Lite clock to 1Hz.
2. Rebuild the design.
3. Use the Quartus Programmer Tool to configure the circuit in the DE10-Lite MAX 10M50 FPGA.
4. Visually verify that the traffic light lamp LEDs meet the functional and timing requirements
5. Visually verify that the status text matches the traffic light lamp LED behaviors.

HINTS

1. The timing diagram shows a repeating pattern of waveforms.
2. Each clock period represents one state.
3. Each output waveform stays high for multiple states based on color.
4. There are 58 total states to generate the traffic control pattern.
5. The machine resets into the reset state called S0 with outputs R1, R2.
6. States S0, S1, and S2 are the three clock periods of R1, R2.

```
-- add these signal declaration in the architecture signal section
signal cnt: integer range 0 to 25000000;
signal clk1Hz : std_logic;

-- add this counter process as a separate process in your architecture
counter: process(rst,clk)
begin
  if rst='0' then cnt<=0;
  elsif rising_edge(clk) then
      cnt <= cnt+1;
      if cnt = 25000000 then
        clk1Hz <= not clk1Hz;
        cnt <= 0;
      end if;
  end if;
end process;

-- modify your register process so that it uses clk1Hz rather than clk
-- example
reg: process(RST,clk1Hz)
begin
  if rising_edge(clk1Hz)
  -- leave the rest of your description
```

Figure 3: Adding a Clock Divider to your Traffic Light VHDL File