DESCRIPTION

This specification describes and defines the basic requirements of the CE1911 simple game. The game must accept user inputs, displays playing elements, keeps score, and has the potential for both winning and losing. Each student designs their own game using creativity and the techniques learned in CE1901 and CE1911.

REQUIREMENTS

- 1. The system must be designed in VHDL and hosted in a DE10-Lite FPGA board.
- 2. The system must use present instructions to the player on reset.
- 3. The system must accept user game control input.
- 4. The system must provide win and lose user feedback.
- 5. The system must use toggle switches or pushbuttons for game play.
- 6. The system must use 7-segment displays for instructions and game play.
- 7. The system can use LEDs for game play.
- 8. The system must be a sequential system with registers, counters, etc.
- 9. The system must operate from DC power or USB supplied power.

TIMELINE

This is a two-week laboratory exercise. Milestones must be demonstrated in each week by each student.

DUE IN	MILESTONE
Week 1	 Storyboard drawings or text of reset behavior and game play behaviors. Use-case diagram and use-case statements. List of DE10-Lite inputs and outputs used for the game. Evidence of initial design work including state machine diagrams, truth tables, user interface 7-segment letter decodings, etc.
Week 2	 Reset and gameplay behavior fully implemented in VHDL. Operational reset and gameplay behavior on DE10-Lite board. Fully commented VHDL code. Completed laboratory documentation including rules of play for the game.

HINTS

- 1. You can have multiple state machines if you want.
- 2. State machines can control other state machines through control signals if needed.
- Decompose your design into functional blocks: SEG7 decoder, counter1, counter2, CLK1Hz, CLK4Hz, etc.
- 4. Multiple VHDL design files are allowed.
- 5. No schematic design is allowed.
- 6. Examples of use-case diagrams and use-case statements can be found in previous laboratories.