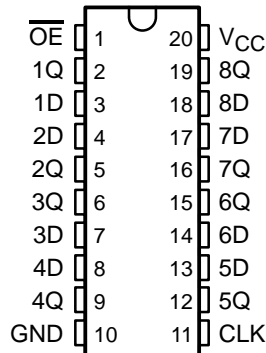


SN54HC374, SN74HC374 OCTAL EDGE-TRIGGERED D-TYPE FLIP-FLOPS WITH 3-STATE OUTPUTS

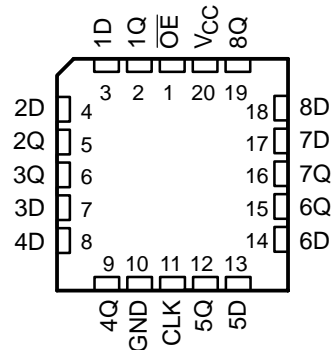
SCLS141D – DECEMBER 1982 – REVISED DECEMBER 2002

- Wide Operating Voltage Range of 2 V to 6 V
- High-Current 3-State True Outputs Can Drive Up To 15 LSTTL Loads
- Eight D-Type Flip-Flops in a Single Package
- Full Parallel Access for Loading
- Low Power Consumption, 80- μ A Max I_{CC}
- Typical $t_{pd} = 14$ ns
- ± 6 -mA Output Drive at 5 V
- Low Input Current of 1 μ A Max

SN54HC374 . . . J OR W PACKAGE
SN74HC374 . . . DB, DW, N, NS, OR PW PACKAGE
(TOP VIEW)



SN54HC374 . . . FK PACKAGE
(TOP VIEW)



description/ordering information

These 8-bit flip-flops feature 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. They are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The eight flip-flops of the 'HC374 devices are edge-triggered D-type flip-flops. On the positive transition of the clock (CLK) input, the Q outputs are set to the logic levels that were set up at the data (D) inputs.

An output-enable (\overline{OE}) input places the eight outputs in either a normal logic state (high or low logic levels) or the high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without interface or pullup components.

ORDERING INFORMATION

TA	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
-40°C to 85°C	PDIP – N	Tube	SN74HC374N	SN74HC374N
	SOIC – DW	Tube	SN74HC374DW	HC374
		Tape and reel	SN74HC374DWR	
	SOP – NS	Tape and reel	SN74HC374NSR	HC374
	SSOP – DB	Tape and reel	SN74HC374DBR	HC374
TSSOP – PW	Tape and reel	SN74HC374PWR	HC374	
-55°C to 125°C	CDIP – J	Tube	SNJ54HC374J	SNJ54HC374J
	CFP – W	Tube	SNJ54HC374W	SNJ54HC374W
	LCCC – FK	Tube	SNJ54HC374FK	SNJ54HC374FK

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

 **TEXAS
INSTRUMENTS**

POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

Copyright © 2002, Texas Instruments Incorporated
On products compliant to MIL-PRF-38535, all parameters are tested unless otherwise noted. On all other products, production processing does not necessarily include testing of all parameters.

SN54HC374, SN74HC374 OCTAL EDGE-TRIGGERED D-TYPE FLIP-FLOPS WITH 3-STATE OUTPUTS

SCLS141D – DECEMBER 1982 – REVISED DECEMBER 2002

description/ordering information (continued)

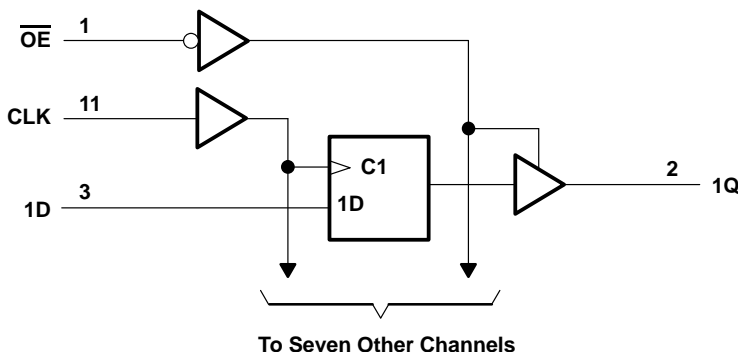
\overline{OE} does not affect the internal operations of the flip-flops. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

FUNCTION TABLE
(each flip-flop)

INPUTS			OUTPUT
\overline{OE}	CLK	D	Q
L	↑	H	H
L	↑	L	L
L	H or L	X	Q_0
H	X	X	Z

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}	–0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) (see Note 1)	±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) (see Note 1)	±20 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	±35 mA
Continuous current through V_{CC} or GND	±70 mA
Package thermal impedance, θ_{JA} (see Note 2):	
DB package	70°C/W
DW package	58°C/W
N package	69°C/W
NS package	60°C/W
PW package	83°C/W
Storage temperature range, T_{stg}	–65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51-7.

SN54HC374, SN74HC374 OCTAL EDGE-TRIGGERED D-TYPE FLIP-FLOPS WITH 3-STATE OUTPUTS

SCLS141D – DECEMBER 1982 – REVISED DECEMBER 2002

recommended operating conditions (see Note 3)

		SN54HC374			SN74HC374			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V _{CC}	Supply voltage	2	5	6	2	5	6	V
V _{IH}	High-level input voltage	V _{CC} = 2 V		1.5	1.5		V	
		V _{CC} = 4.5 V		3.15	3.15			
		V _{CC} = 6 V		4.2	4.2			
V _{IL}	Low-level input voltage	V _{CC} = 2 V			0.5	0.5	V	
		V _{CC} = 4.5 V			1.35	1.35		
		V _{CC} = 6 V			1.8	1.8		
V _I	Input voltage	0		V _{CC}	0		V _{CC}	V
V _O	Output voltage	0		V _{CC}	0		V _{CC}	V
Δt/Δv	Input transition rise/fall time	V _{CC} = 2 V			1000	1000	ns	
		V _{CC} = 4.5 V			500	500		
		V _{CC} = 6 V			400	400		
T _A	Operating free-air temperature	-55		125	-40		85	°C

NOTE 3: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V _{CC}	T _A = 25°C		SN54HC374		SN74HC374		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	
V _{OH}	V _I = V _{IH} or V _{IL}	I _{OH} = -20 μA	2 V	1.9	1.998		1.9		1.9	V
			4.5 V	4.4	4.499		4.4		4.4	
			6 V	5.9	5.999		5.9		5.9	
		I _{OH} = -6 mA	4.5 V	3.98	4.3		3.7		3.84	
		I _{OH} = -7.8 mA	6 V	5.48	5.8		5.2		5.34	
V _{OL}	V _I = V _{IH} or V _{IL}	I _{OL} = 20 μA	2 V		0.002	0.1		0.1	0.1	V
			4.5 V		0.001	0.1		0.1	0.1	
			6 V		0.001	0.1		0.1	0.1	
		I _{OL} = 6 mA	4.5 V		0.17	0.26		0.4	0.33	
		I _{OL} = 7.8 mA	6 V		0.15	0.26		0.4	0.33	
I _I	V _I = V _{CC} or 0		6 V		±0.1	±100		±1000	±1000	nA
I _{OZ}	V _O = V _{CC} or 0		6 V		±0.01	±0.5		±10	±5	μA
I _{CC}	V _I = V _{CC} or 0, I _O = 0		6 V			8		160	80	μA
C _i			2 V to 6 V		3	10		10	10	pF

SN54HC374, SN74HC374 OCTAL EDGE-TRIGGERED D-TYPE FLIP-FLOPS WITH 3-STATE OUTPUTS

SCLS141D – DECEMBER 1982 – REVISED DECEMBER 2002

timing requirements over recommended operating free-air temperature range (unless otherwise noted)

	V _{CC}	T _A = 25°C		SN54HC374		SN74HC374		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
f _{clock} Clock frequency	2 V	6		4		5		MHz
	4.5 V	30		20		24		
	6 V	35		24		28		
t _w Pulse duration, CLK high or low	2 V	80		120		100		ns
	4.5 V	16		24		20		
	6 V	14		20		17		
t _{su} Setup time, data before CLK↑	2 V	100		150		125		ns
	4.5 V	20		30		25		
	6 V	17		25		21		
t _h Hold time, data after CLK↑	2 V	10		13		12		ns
	4.5 V	5		5		5		
	6 V	5		5		5		

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC}	T _A = 25°C			SN54HC374		SN74HC374		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f _{max}			2 V	6	12		4		5	MHz	
			4.5 V	30	60		20		24		
			6 V	35	70		24		28		
t _{pd}	CLK	Any Q	2 V		63	180		270		225	ns
			4.5 V		17	36		54		45	
			6 V		15	31		46		38	
t _{en}	\overline{OE}	Any Q	2 V		60	150		225		190	ns
			4.5 V		16	30		45		38	
			6 V		14	26		38		32	
t _{dis}	\overline{OE}	Any Q	2 V		36	150		225		190	ns
			4.5 V		17	30		45		38	
			6 V		16	26		38		32	
t _t		Any Q	2 V		28	60		90		75	ns
			4.5 V		8	12		18		15	
			6 V		6	10		15		13	



SN54HC374, SN74HC374 OCTAL EDGE-TRIGGERED D-TYPE FLIP-FLOPS WITH 3-STATE OUTPUTS

SCLS141D – DECEMBER 1982 – REVISED DECEMBER 2002

switching characteristics over recommended operating free-air temperature range, $C_L = 150 \text{ pF}$ (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC}	T _A = 25°C			SN54HC374		SN74HC374		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f _{max}			2 V	6	12			5		MHz	
			4.5 V	30	60			24			
			6 V	35	70			28			
t _{pd}	CLK	Any Q	2 V		80	230	345		290	ns	
			4.5 V		22	46	69		58		
			6 V		19	39	58		49		
t _{en}	$\overline{\text{OE}}$	Any Q	2 V		70	200	300		250	ns	
			4.5 V		25	40	60		50		
			6 V		22	34	51		43		
t _t		Any Q	2 V		45	210	315		265	ns	
			4.5 V		17	42	63		53		
			6 V		13	36	53		45		

operating characteristics, T_A = 25°C

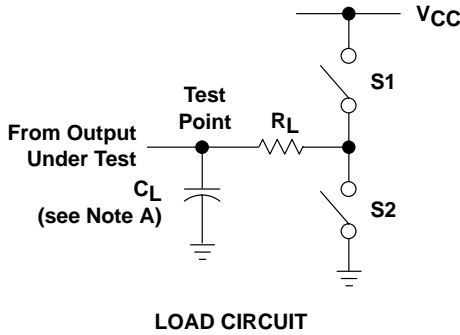
PARAMETER	TEST CONDITIONS	TYP	UNIT
C _{pd} Power dissipation capacitance per flip-flop	No load	100	pF



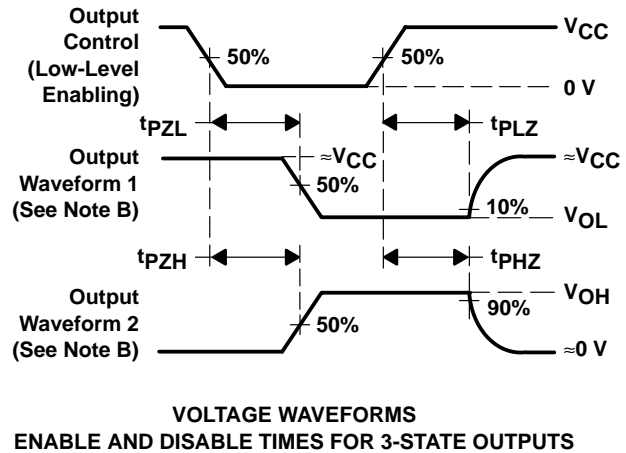
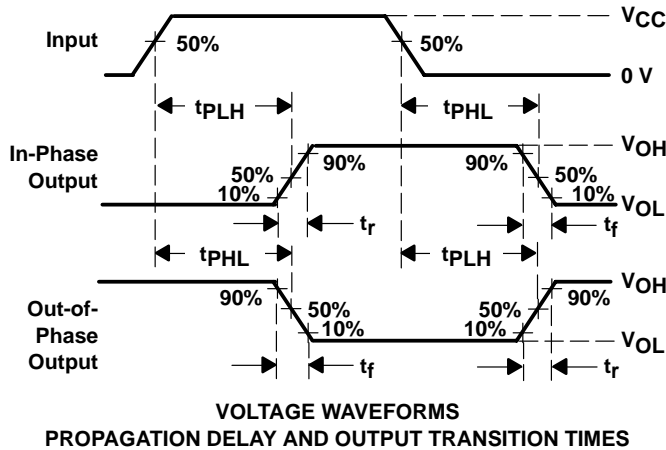
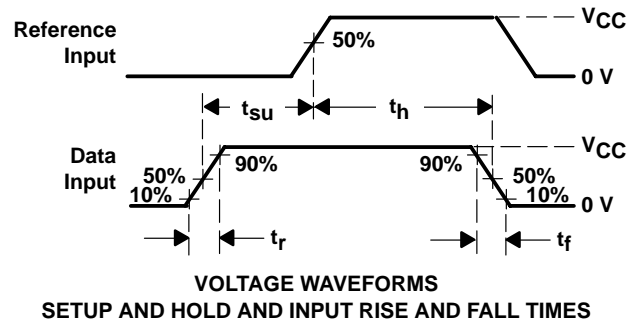
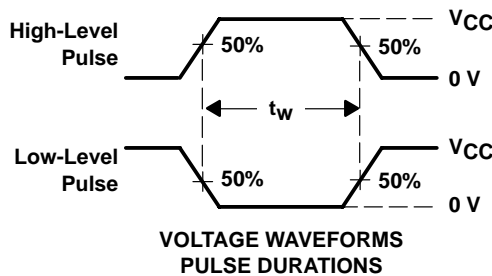
SN54HC374, SN74HC374 OCTAL EDGE-TRIGGERED D-TYPE FLIP-FLOPS WITH 3-STATE OUTPUTS

SCLS141D – DECEMBER 1982 – REVISED DECEMBER 2002

PARAMETER MEASUREMENT INFORMATION



PARAMETER	R_L	C_L	S1	S2
t_{en}	1 k Ω	50 pF or 150 pF	Open	Closed
			Closed	Open
t_{dis}	1 k Ω	50 pF	Open	Closed
			Closed	Open
t_{pd} or t_t	—	50 pF or 150 pF	Open	Open



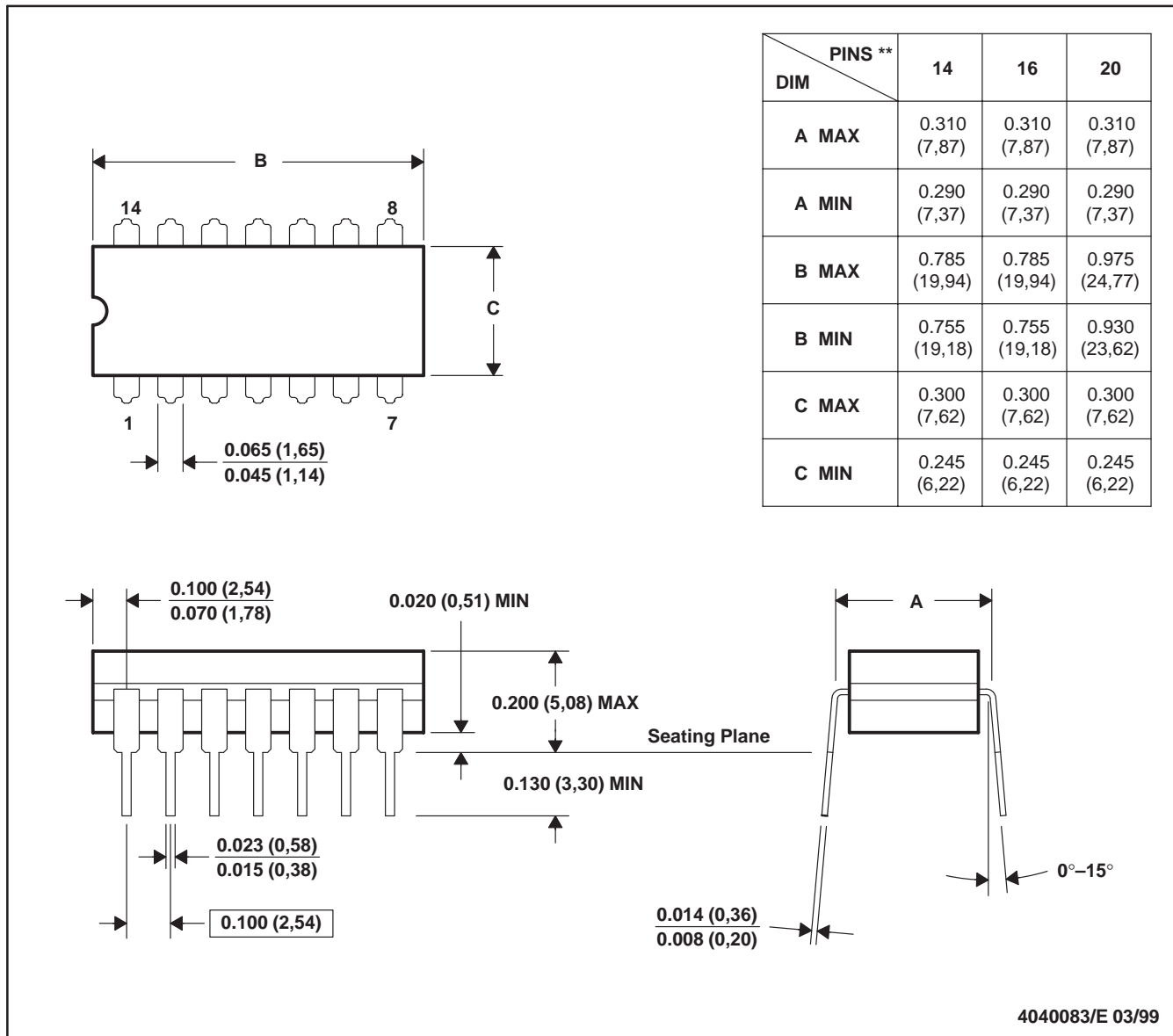
- NOTES: A. C_L includes probe and test-fixture capacitance.
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 C. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: $PRR \leq 1$ MHz, $Z_O = 50 \Omega$, $t_r = 6$ ns, $t_f = 6$ ns.
 D. For clock inputs, f_{max} is measured when the input duty cycle is 50%.
 E. The outputs are measured one at a time with one input transition per measurement.
 F. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 G. t_{PZL} and t_{PZH} are the same as t_{en} .
 H. t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 1. Load Circuit and Voltage Waveforms

J (R-GDIP-T**)

CERAMIC DUAL-IN-LINE

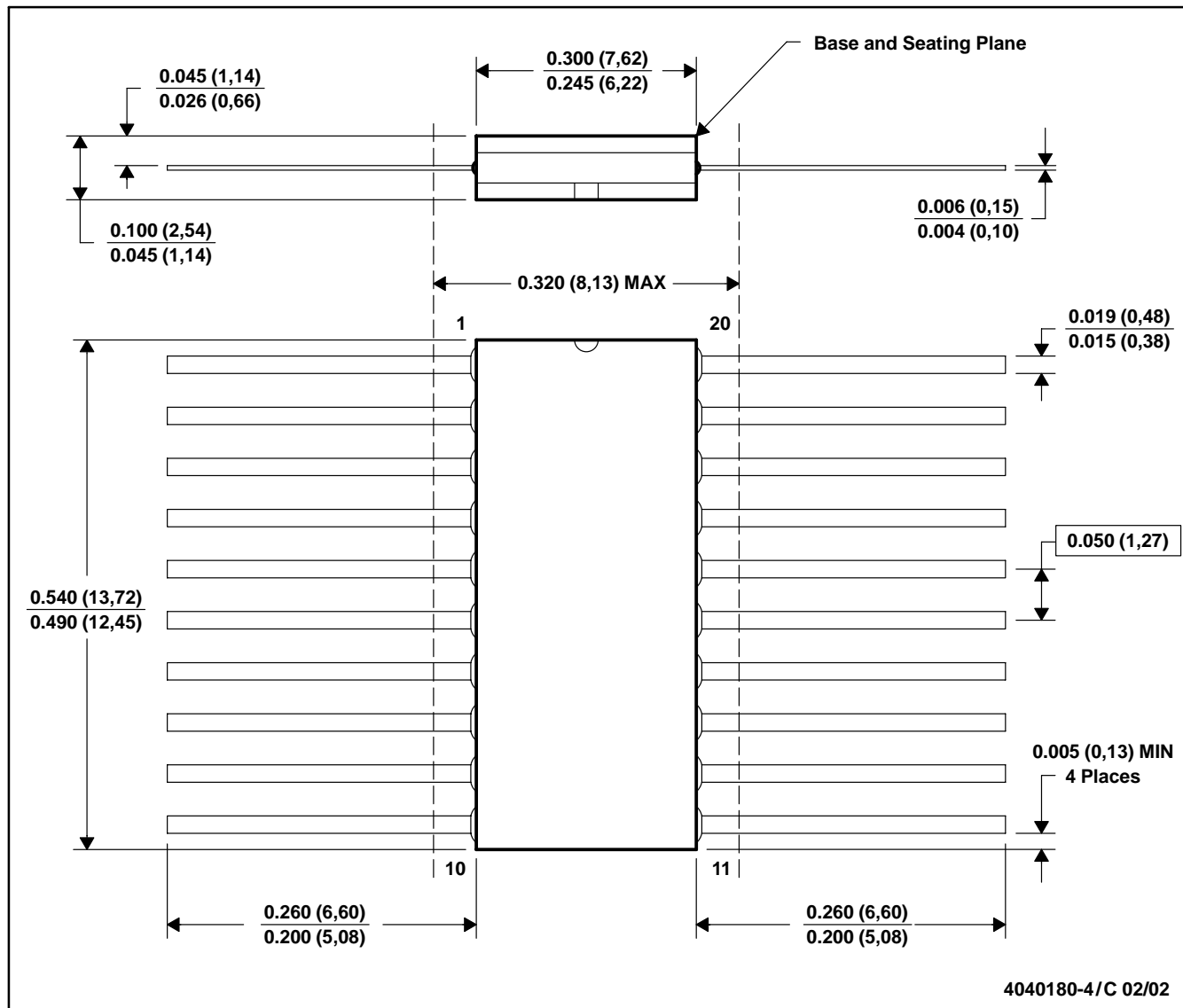
14 LEADS SHOWN



- NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.
 C. This package is hermetically sealed with a ceramic lid using glass frit.
 D. Index point is provided on cap for terminal identification.
 E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, and GDIP1-T20

W (R-GDFP-F20)

CERAMIC DUAL FLATPACK



- NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.
 C. This package can be hermetically sealed with a ceramic lid using glass frit.
 D. Index point is provided on cap for terminal identification only.

FK (S-CQCC-N**)

LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN

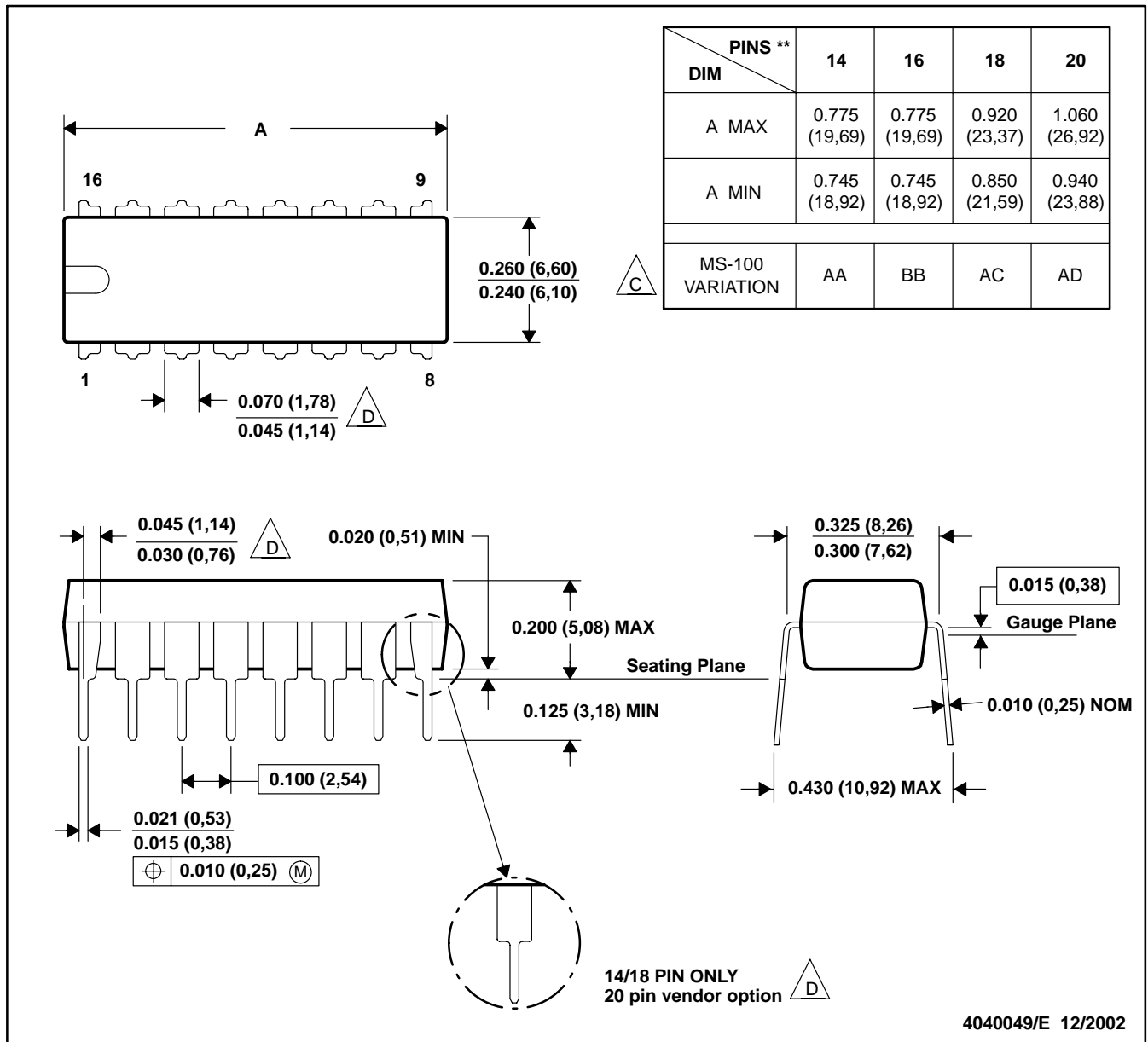


- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package can be hermetically sealed with a metal lid.
 - D. The terminals are gold plated.
 - E. Falls within JEDEC MS-004

N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN

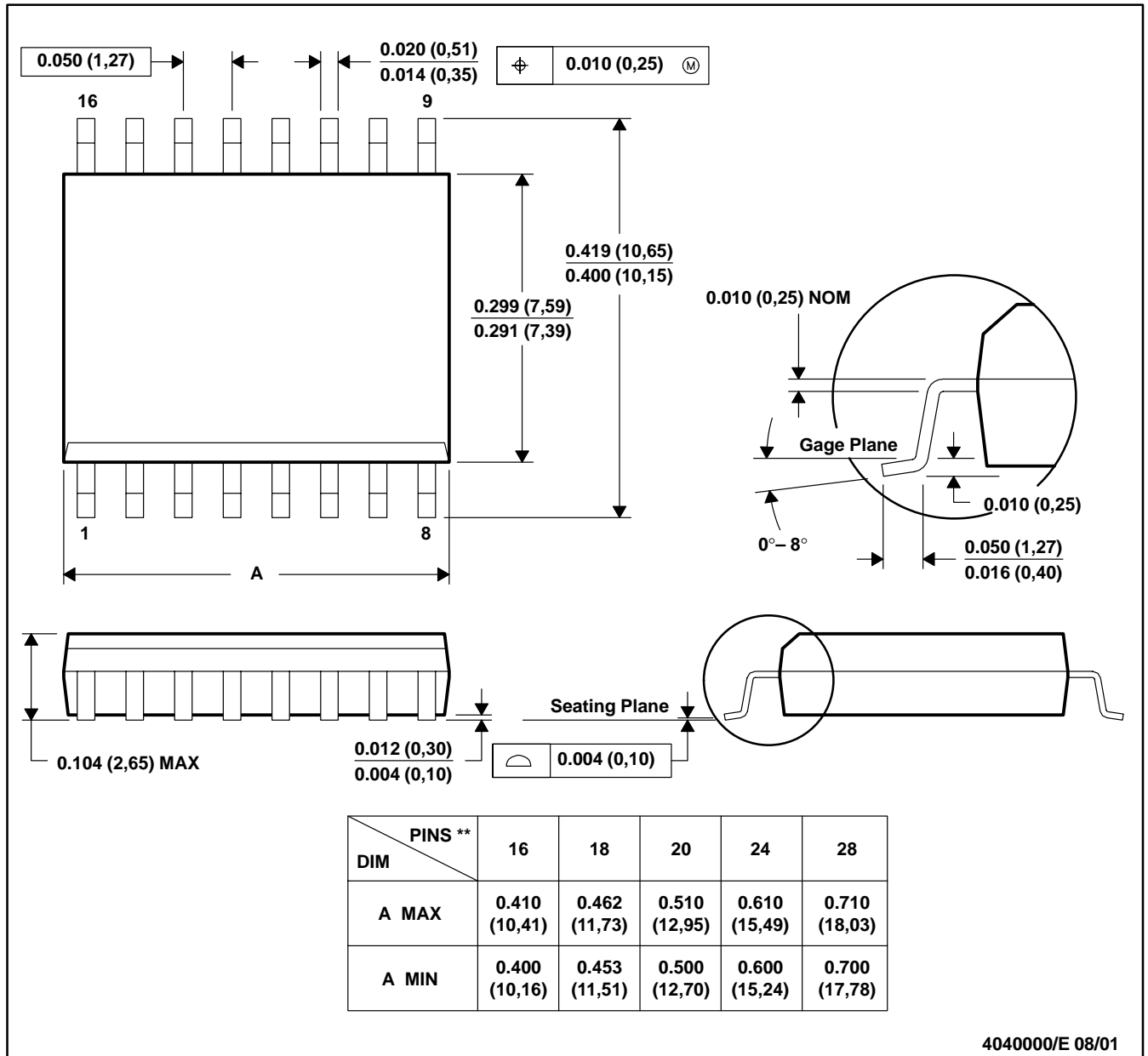


- NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.
 (C) Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 (D) The 20 pin end lead shoulder width is a vendor option, either half or full width.

DW (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

16 PINS SHOWN

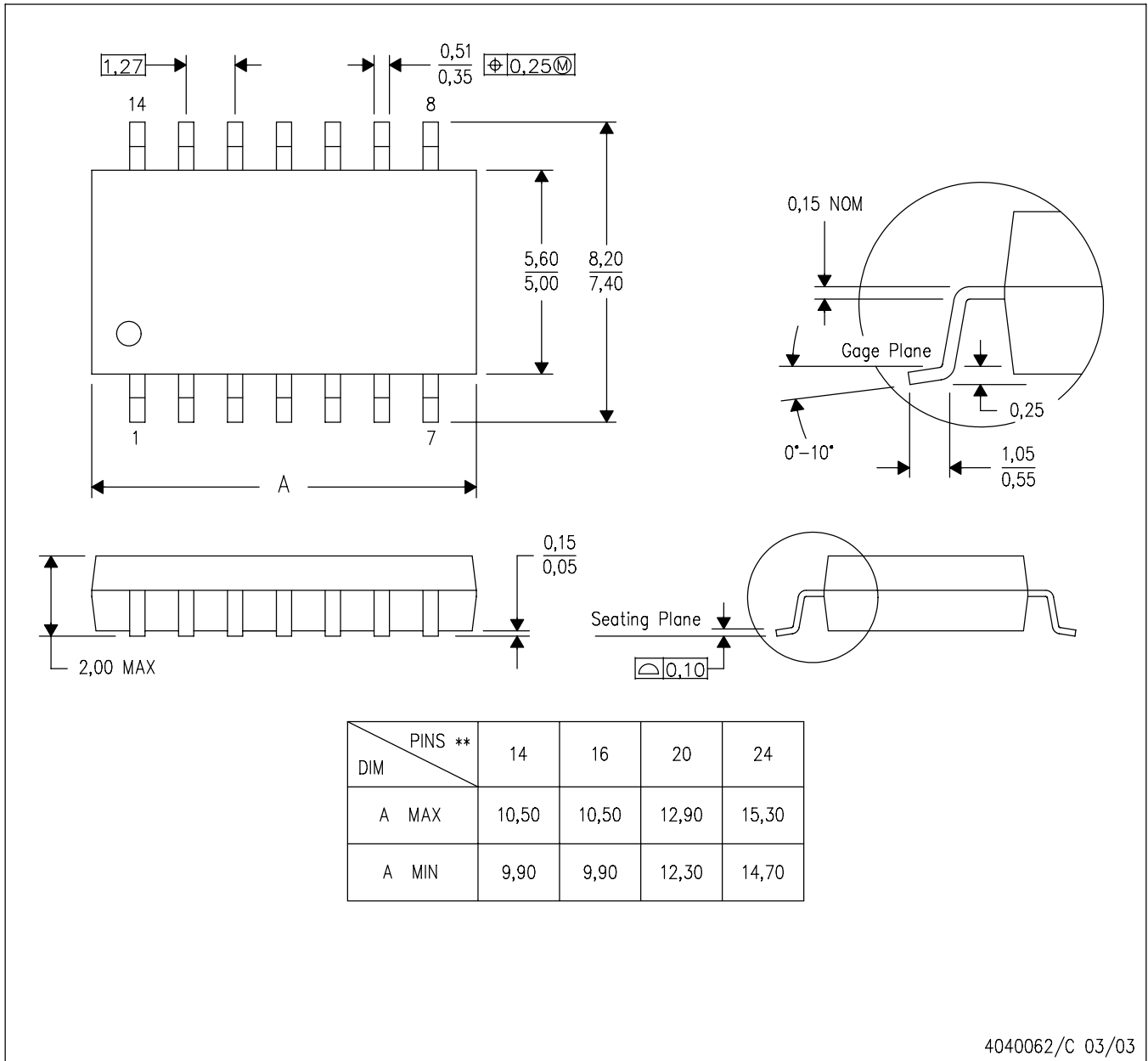


4040000/E 08/01

- NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
 D. Falls within JEDEC MS-013

NS (R-PDSO-G**)
 14-PIN SHOWN

PLASTIC SMALL-OUTLINE PACKAGE



4040062/C 03/03

- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

DB (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

28 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-150

PW (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14 PINS SHOWN



4040064/F 01/97

- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-153

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Mailing Address:

Texas Instruments
Post Office Box 655303
Dallas, Texas 75265