PIPELINED PROCESSORS

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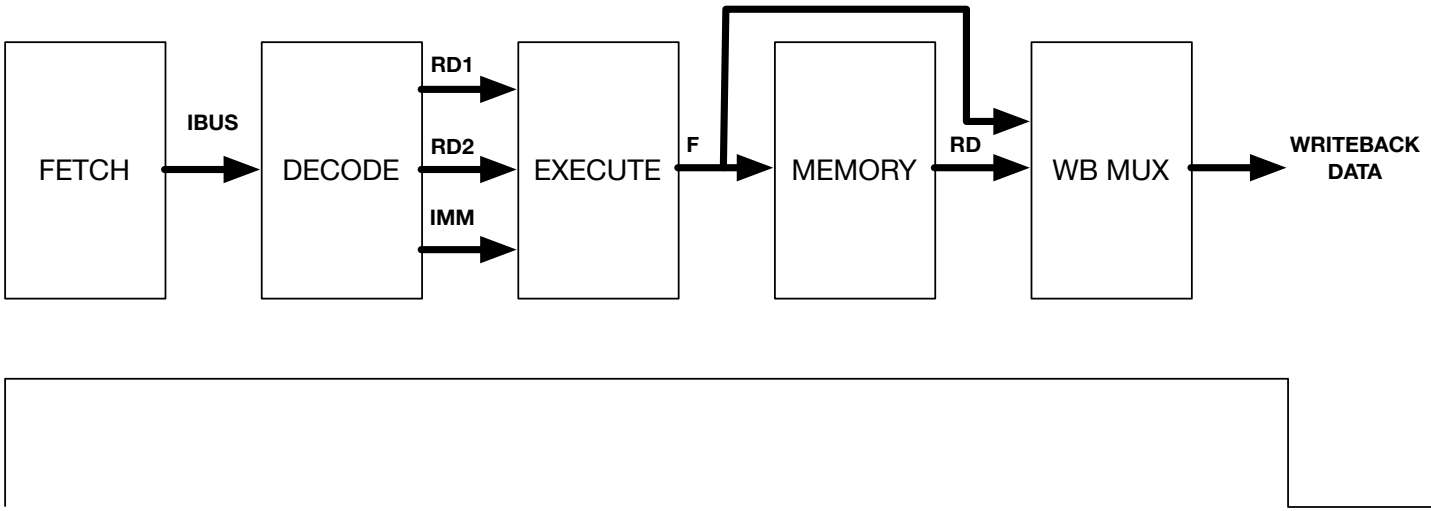
SINGLE CYCLE PROCESSOR

- Clock period set by memory load instructions.
- Instructions that don't use memory are penalized.



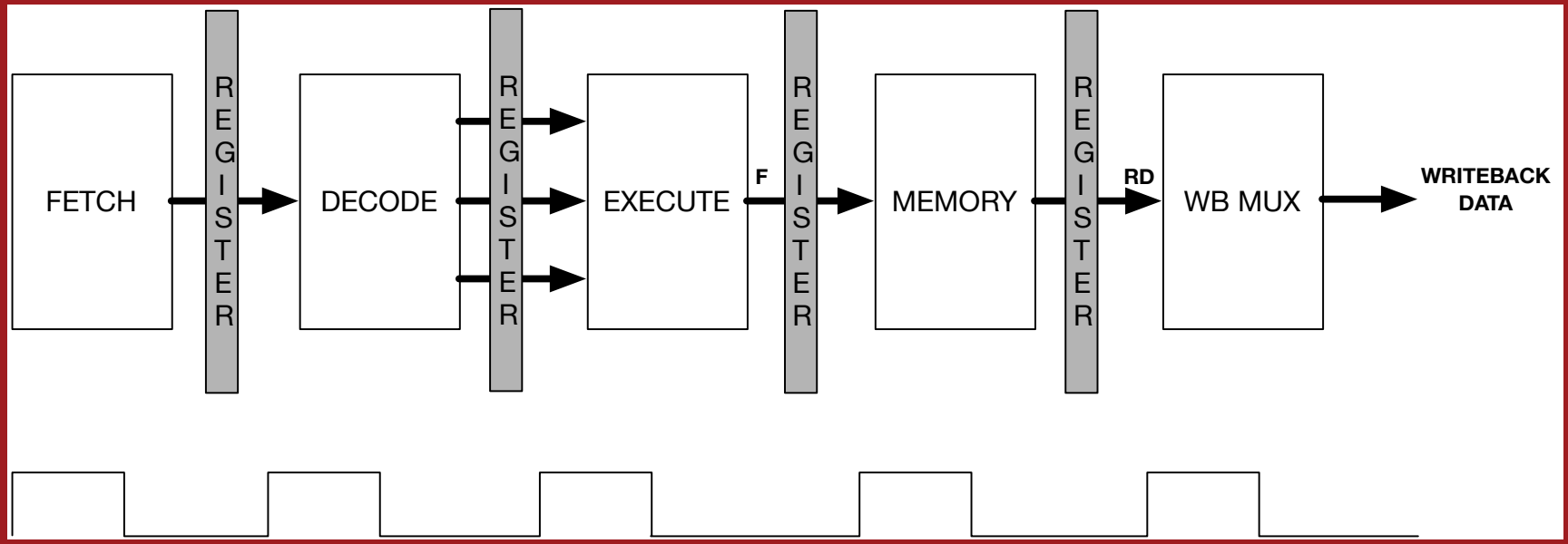
SINGLE CYCLE PROCESSOR

- Advantages
  - Simple
  - Control is quite easy
- Disadvantages
  - LDR sets clock period
  - All instructions delay
  - Each circuit stage only active for one delay in an instruction's execution time

PIPELINED PROCESSOR

- Why not separate circuit with sample registers?
- Why not use a faster clock period set by slowest circuit stage?
- Why hold instruction binary number just in fetch?
- Why not reuse each stage on each clock period?
- Can a train of instructions pulsing through the circuit be sustained to keep utilization high?

PIPELINED PROCESSOR



MSOE UNIVERSITY

PIPELINED PROCESSOR

- Advantages
  - Five instructions in flight.
  - Circuits highly utilized.
  - Speedup = 5
- Disadvantages
  - More space needed
  - Control more complex
  - Hazards stall the pipeline