1. Suppose your team is re-engineering an existing scalar pipelined processor so that it becomes a four-way superscalar processor that permits three integer instructions *or* one load-store instruction to dispatch per dispatch time unit. The integer pipes are clocked as two circuit stages each (because multiplication and division are implemented within these pipes) while the load-store circuit is clocked as a three-stage circuit. The pre-execution circuit consists of a fetch stage, a decode stage, and a dispatch stage that contains an 8-instruction dispatch buffer. Instructions dispatch in-order and no out-of-order techniques are included in the design. Results from integer instructions write simultaneously to the register file in the single write-back stage.

    a. **Draw** the organization suggested by the design information. **Use** a tool like Microsoft Visio to draw a production level diagram rather than a hand sketch.
    b. **Explain** why load-store instructions cannot dispatch simultaneously with integer instructions.
    c. **Estimate** the processor IPC on long sections of code that do not contain control hazards. In other words, would you expect IPC to be 0.5, 1, between 3 and 4? **Explain** your answer.

2. **Explain** why superscalar processing could be added to any existing processor without having to recompile source code. **In other words**, older executables downloaded from the internet for a non-superscalar version of the instruction set architecture are able to be run on a superscalar version. Why?

3. NVIDIA released it first internally designed microprocessor – a 64-bit version of the ARM instruction set architecture code named DENVER – this past year. **Read** the IEEE Micro paper on Denver and answer this questions with diagrams and short essays.

    a. **Describe** the degree of superscalarism. **Include** information about the parallel pipes and any limitations on dispatch to the parallel pipes. Is there any unique feature about the integer or load-store pipes that make them more useful during dispatch?
    b. **State** the misprediction penalty for DENVER.
    c. **Briefly** describe DENVER dynamic code optimization. What does it do? How does it improve speculative branch prediction? How does it improve pipeline efficiency?

DELIVERABLES

- **Complete** your work in electronic format.
- **Submit** an electronic PDF by email to the instructor by Friday of Week 7.