CE4940 FALL 2016 HOMEWORK HW1

1. **Calculate** the saturation current of an NMOS for three different VGS values: 1.8V, 3.3V, and 5V. These threecvoltages are typical power supply voltages (logic-1 values) for CMOS circuits. **Use** these CMOS process parameters: un*COX = 100uA/V*V, W=20nm, L=20nm, Vt = 0.48V. **Sketch** the I-V curves for this NMOS based on your three calculated values (you will have three curves on the plot.
2. **Repeat** your work in problem 1 using a new value of Vt = 1.1V. **Explain** the effect of this new Vt on the I-V curves.
3. **Create** a neatly drawn transistor-level hand-sketch of a four-input passive-pullup NOR gate.
4. **Create** a neatly drawn transistor-level hand-sketch of a three-input passive-pullup AND gate.
5. **Create** a neatly drawn transistor-level hand-sketch of a circuit that implements AND-OR logic equation F(ABC) = AB + C using passive-pullup. The solution to this problem can be done with only four transistors. **Hint:** remember the rules for OR and AND behavior in the N-plane. Combine series and parallel resistors to form the equation and then use a second stage to remove the complement.