CE4940 VLSI DESIGN TECHNIQUES
WEEK 3 LABORATORY

LABORATORY LEARNING OBJECTIVES

- **Design** RTL inverters to meet voltage transfer characteristic specifications.
- **Simulate** design results using PSPICE.

LABORATORY REQUIREMENTS

1. **Work** these exercises alone. **Consult** the instructor and classmates for help if needed.
2. **Complete** each design and simulation during your study time and lab time.
3. **Submit** a **formal** PDF laboratory report by 5 pm on Friday of the week the laboratory is due. **Create** your report in Microsoft Word (or other appropriate editor) and print to PDF.
4. **Include** these items in your report:
    a. **Abstract:** The abstract section describes the work completed in the laboratory. It should be a short summary designed to inform a reader of what they can expect to read more deeply about in the lab report.
    b. **Introduction:** The introduction section describes the basic circuits that will be designed or analyzed in the laboratory. Circuit diagrams are presented and key equations are derived.
    c. **Designs:** Each laboratory design includes its own section for derivations, final circuit diagrams, SPICE simulation text files, SPICE simulation plots, and a discussion section that describes how you know the solution is correct.

LABORATORY EXERCISES

1. **Design** an NMOS pull-down, passive pullup inverter (RTL) with **VOL = 0.45V** if KP = 200 $\mu A/V^2$, VT = 0.75V, W/L = 5, L=2U and VDD = 5V. meet a VOL specification.
2. **Design** an NMOS RTL inverter with **VOL = 0.25V** if KP = 167 $\mu A/V^2$, VTN = 0.68V, W/L = 2, L=0.5U, and VDD = 3.3V.
3. **Design** an NMOS RTL inverter with **VOL = 0.1V** if KP = 167 $\mu A/V^2$, VTN = 0.9V, W/L = 1, L=0.5U, and VDD = 5V.