CE4940 VLSI DESIGN TECHNIQUES
WEEK 3 LABORATORY

LABORATORY LEARNING OBJECTIVES

- **Design** RTL logic gates and complex logic to meet voltage transfer characteristic specs.
- **Simulate** design results using PSPICE.

LABORATORY REQUIREMENTS

1. **Work** these exercises alone. **Consult** the instructor and classmates for help if needed.
2. **Complete** each design and simulation during your study time and lab time.
3. **Submit** a **formal** PDF laboratory report by 5 pm on Friday of the laboratory week. **Create** your report in Microsoft Word (or other appropriate editor) and print to PDF.
4. **Include** these items in your report:
    a. **Abstract**: The abstract section describes the work completed in the laboratory. It should be a short summary designed to inform the reader of what they can expect to read more deeply about in the lab report.
    b. **Introduction:** The introduction section describes the basic circuits that will be designed or analyzed in the laboratory. Circuit diagrams are presented and key equation results are listed.
    c. **Designs:** Each laboratory design includes its own section for derivations, final circuit diagrams, SPICE simulation text files, SPICE simulation plots, and a discussion section that describes how you know the solution is correct.

LABORATORY EXERCISE

Use the Agilent 0.5U process model to guide the design and SPICE simulation of a family of VOL=0.2V RTL 2-input logic gates that includes NAND2, NOR2, XNOR, AND2, OR2, and XOR2. **Assume** a VDD of 5V, a constant transistor length set by the process name, and a constant resistor mask image of 4.7KΩ.

- **Remember**: Scale transistor widths based on the reference inverter design.
- **Remember:** Good simulation includes both voltage and time domains.
- **Remember**: XOR is true if exactly one input is true.
- Time domain simulation hint: form a binary number line on inputs A and B by setting the A pulse period and width to be twice the B pulse.