CE4940 VLSI DESIGN TECHNIQUES
WEEK 5 LABORATORY

LABORATORY LEARNING OBJECTIVES

- **Design** CMOS logic gates and complex logic to meet voltage transfer characteristic specs.
- **Simulate** design results using PSPICE.

LABORATORY REQUIREMENTS

1. **Work** these exercises alone. **Consult** the instructor and classmates for help if needed.
2. **Complete** each design and simulation during your study time and lab time.
3. **Submit** a **formal** PDF laboratory report by 5 pm on Friday of the following week. **Create** your report in Microsoft Word (or other appropriate editor) and print to PDF.
4. **Include** these items in your report:
    a. **Abstract**: The abstract section describes the work completed in the laboratory. It should be a short summary designed to inform the reader of what they can expect to read more deeply about in the lab report.
    b. **Introduction:** The introduction section describes the basic circuits that will be designed or analyzed in the laboratory. Circuit diagrams are presented and key equation results are listed.
    c. **Designs:** Each laboratory design includes its own section for derivations, final circuit diagrams, SPICE simulation text files, SPICE simulation plots, and a discussion section that describes how you know the solution is correct.

LABORATORY EXERCISE

Use the data in Table 1 to guide the design and SPICE simulation of a family of CMOS logic gates that includes NAND2, NOR2, XNOR, AND2, OR2, and XOR2. **Assume** an ideal switching threshold is the design goal.

- **Remember**: Scale n-input gate transistor widths based on the reference inverter design.
- **Remember:** Good simulation includes both voltage and time domains for the inverter and time domain simulations for the remaining gates.
- **Remember**: XOR is true if exactly one input is true.
- Time domain simulation hint: form a binary number line on inputs A and B by setting the A pulse period and width to be twice the B pulse.

TABLE 1: PARAMETERS FOR USE IN CMOS DESIGN

NMOS	VTO = 0.6V	KP = 60 µA/V^2	L = 0.8µm
PMOS	VTO = -0.7V	KP=25 µA/V^2	L=0.8µm
VDD	3.3V		