CE4940 VLSI DESIGN TECHNIQUES
WEEK 7 LABORATORY

LABORATORY LEARNING OBJECTIVES

- **Design** Pseudo-NMOS logic gates and complex logic to meet VTC specificiations.
- **Compare** and **contrast** power and space requirements of RTL, CMOS, and Pseudo-NMOS.
- **Simulate** design results using PSPICE.

LABORATORY REQUIREMENTS

1. **Work** these exercises alone. **Consult** the instructor and classmates for help if needed.
2. **Complete** each design and simulation during your study time and lab time.
3. **Submit** a **formal** PDF laboratory report by 5 pm on Friday of the following week. **Create** your report in Microsoft Word (or other appropriate editor) and print to PDF.
4. **Include** these items in your report:
    a. **Abstract**: The abstract section describes the work completed in the laboratory. It should be a short summary designed to inform the reader of what they can expect to read more deeply about in the lab report.
    b. **Introduction:** The introduction section describes the basic circuits that will be designed or analyzed in the laboratory. Circuit diagrams are presented and key equation results are listed.
    c. **Designs:** Each laboratory design includes its own section for derivations, final circuit diagrams, SPICE simulation text files, SPICE simulation plots, and a discussion section that describes how you know the solution is correct.

LABORATORY EXERCISE

Psuedo-NMOS gates replace the PMOS transistors in the CMOS p-plane with exactly one always-on PMOS device. This technique has both advantages and disadvantages when compared and contrasted against RTL and CMOS configuration. The VTC design point for Pseudo-NMOS is V_{OL} and the balance equation can be obtained by noting that the NMOS device is non-saturated and the PMOS device is saturated when the output is pulled near zero for V_{OL}. **Use** the data in Table 1 of the last laboratory to guide your paper design and SPICE simulation of a family of Pseudo-NMOS logic gates that includes NAND2, NOR2, XNOR, AND2, OR2, and XOR2. **Assume** that VOL=0.4 is the VTC design goal. **Complete** a comparison and contrast exercise between the power and space requirements of RTL, CMOS, and Pseudo-NMOS as part of your discussion section in your laboratory report. **Assume** the RTL reference inverter achieves the same V_{OL}=0.4V when completing the comparison and contrast exercise.

- **Assume** that interconnect area will be ignored. In other words, all components are built immediately next to each other during fabrication with no wire length.
- **Assume** transistor area is calculated as simply W*L.
- **Note** that resistors can be fabricated on semiconductor as a line of polysilicon material with a specified length and width giving a total area of W*L. The equation used to calculate resistance is: $R = R_{sheet} * \left(\frac{W}{L}\right) \Omega$. **Assume** that the fabrication sheet resistance is 30Ω and that length is fixed at the same constant channel length of the transistors.
- **Remember:** Good simulation includes both voltage and time domains for the inverter and time domain simulations for the remaining gates.