# CE4940 VLSI DESIGN TECHNIQUES
# WEEK 8 LABORATORY

**LABORATORY LEARNING OBJECTIVES**

- **Design** CMOS and Pseudo-NMOS memory latches to meet VTC specificiations.
- **Compare** and **contrast** power and space requirements of CMOS, and Pseudo-NMOS.
- **Simulate** design results using PSPICE.

**LABORATORY REQUIREMENTS**

1. **Work** these exercises alone. **Consult** the instructor and classmates for help if needed.
2. **Complete** each design and simulation during your study time and lab time.
3. **Submit** a **formal** PDF laboratory report by 5 pm on Friday of the following week. **Create** your report in Microsoft Word (or other appropriate editor) and print to PDF.
4. **Include** these items in your report:
    a. **Abstract**: The abstract section describes the work completed in the laboratory. It should be a short summary designed to inform the reader of what they can expect to read more deeply about in the lab report.
    b. **Introduction:** The introduction section describes the basic circuits that will be designed or analyzed in the laboratory. Circuit diagrams are presented and key equation results are listed.
    c. **Designs:** Each laboratory design includes its own section for derivations, final circuit diagrams, SPICE simulation text files, SPICE simulation plots, and a discussion section that describes how you know the solution is correct.

**LABORATORY EXERCISE**

Memory latch circuits use output-to-input feedback to create memory behavior. The SR latch is the basic memory element introduced in digital logic. This basic element can be expanded by adding additional gates to provide modified behavior. For example, SR latches have an input condition that is “not allowed” because it does not make logical sense. D-latches overcome this limitation and are a simple expansion from the SR latch. And, level-sensitive enable is easily added so that memory can selectively sample inputs. These basic memory circuits have been reviewed in lecture and now will be implemented in both CMOS and Pseudo-NMOS.

- **Assume VDD=5V** supply level. **Use** the TSMC 0.25U process models to design both the CMOS and Pseudo-NMOS reference inverters. CMOS should achieve the ideal switching threshold of ½ VDD and Pseudo-NMOS should achieve VOL=0.5V.
- **Design** and **simulate** the D-latch with enable in both CMOS and Pseudo-NMOS.
- **Estimate** the total area required for each design if interconnect area is ignored. In other words, you are simply summing the rectangular transistor areas.
- **Compare** and **contrast** static power consumption.
- **Remember** that good simulation verifies both VTC and transient behaviors.