CE4940 VLSI DESIGN TECHNIQUES
WEEK 9 LABORATORY

LABORATORY LEARNING OBJECTIVES

- **Design** CMOS device level layout diagrams for logic gates using Electric.
- **Simulate** design results using the Electric ALS.

LABORATORY REQUIREMENTS

1. **Work** these exercises alone. **Consult** the instructor and classmates for help if needed.
2. **Complete** each design and simulation during your study time and lab time.
3. **Submit** a **formal** PDF laboratory report by 5 pm on Friday of the following week. **Create** your report in Microsoft Word (or other appropriate editor) and print to PDF.
4. **Include** these items in your report:
    a. **Abstract**: The abstract section describes the work completed in the laboratory. It should be a short summary designed to inform the reader of what they can expect to read more deeply about in the lab report.
    b. **Introduction:** The introduction section describes the basic circuits that will be designed or analyzed in the laboratory. Circuit diagrams are presented and key equation results are listed.
    c. **Designs:** Each laboratory design includes its own section for derivations, final circuit diagrams, SPICE simulation text files, SPICE simulation plots, and a discussion section that describes how you know the solution is correct.

LABORATORY EXERCISE

Layout diagrams show the transistor level devices as rectangular areas of materials. These areas represent the masks that will be used to during the fabrication etching, implantation, and growth phases.

- **Complete** layout diagrams for NAND, NOR, AND, and OR gates using the Mosis CMOS process in Electric (MOCMOS).
- **Verify** logical behavior using the Electric ALS simulator.