Undergraduate Research Project
Scalable Superscalar MIPS Processor Core

Abstract:
Modern microprocessor architectures extend pipelined micro-architecture in a number of ways to exploit instruction-level parallelism (ILP) and thread-level parallelism (TLP). Deep pipelines, superscalar pipelines, out-of-order instruction execution, instruction reordering and speculative execution are example techniques exploiting ILP. The goal of this project is a scalable superscalar MIPS processor core that can be placed into Altera field-programmable gate arrays.

Requirements

- MIPS32 ISA including core instructions, multiply, divide, and floating point math
- Generic width arithmetic circuit to allow for 8, 16, and 32 bit processors
- 3-way superscalar design with two integer and one floating point pipeline
- development of a unique algorithm for out-of-order instruction dispatch to handle hazards
- development of a unique energy-efficient power management algorithm for multiple pipelines
- memory-mapped IO subsystem to allow user input and output

Deliverables

- MIPS core design files written in VHDL
- Pre-compiled MIPS cores for 8, 16, and 32 bit processors
- Simulation and test plans
- Simulation and test results
- User manual
- Conference ready poster describing the work completed
- Submission of a paper to a research-oriented student or professional conference

Enrollment:

- Prerequisite: CE2930 with a grade of B or better
- Co-requisite: CE4930 or permission of instructor
- Level: Junior or Senior standing at MSOE
- GPA: Cummulative GPA >=3.2
- Approval: EECS Department Chair

Learning Outcomes:

- Create a research project management timeline.
- Conduct a bibliometric search of the research literature.
- Describe how superscalar architectures improve throughput.
- Describe advanced hazard management techniques.
- Describe the structure of a modern FPGA and limitations it imposes on processor core design.
- Develop algorithms that extend current science into new directions.
- Implement architectures as scalable circuitry in FPGAs
- Document and present peer-reviewed research to the community.

Credits:
The student selected for this project must enroll and make acceptable progress in each of UR4981, UR4982, and UR4983. Successful completion of all three courses with a grade of B or higher will result in 6 credits that will be counted toward two CE technical electives.

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