# MSOE EECS Department
# CE-1901: Week 6 Lab Grading Checklist
# Dr. Yoder Name:

| Item | Points |
|---|---|
| Prelab 2 truth table and K-map | / 4 |
| Prelab 2 design, VHDL, RTL, simulation, and demonstration | / 4 |
| Prelab 3 design, VHDL, RTL, simulation, and demonstration | / 4 |
| Prelab 4 design, VHDL, RTL, simulation, and demonstration | / 4 |
| In-lab Exercise 2 design, VHDL, RTL, simulation, and demonstration (This is an individual exercise) | / 4 |
| **Total** | / 20 |

- ***Staple*** this lab cover sheet on top of all the materials you are submitting.
- Submit your work in the ***order*** listed above.
- Your lab packet is due by 9 AM on the day after the lab is performed. You may do your (late) demonstration after submitting your lab packet if necessary. There is a 1 point per day late penalty on the demo. The maximum late penalty for the report+demo per day is 2 points. Leave your submitted lab packet on the bulletin board outside my office door or submit your packet to me during the laboratory.

Acknowledgement: Original checklist by Dr. Durant and Dr. Meier