# MSOE EECS Department
# CE-1901: Week 7 Lab Grading Checklist
# Dr. Yoder Name:

| Item | Points |
|---|---|
| Prelab 2 VHDL : MUX41 structural VHDL, RTL, simulation | / 4 |
| Prelab 3 VHDL: MUX81 structural VHDL, RTL, simulation | / 4 |
| Prelab 4: VHDL: MUX161 structural VHDL, RTL, simulation | / 4 |
| In-class exercise: AB < BC designed (e.g. VHDL) using the MUX81 component | / 3 |
| In-class exercise: AB < BC demoed | / 3 |
| Meets submission requirements below | / 2 |
| **Total** | / 20 |

- ***Staple*** this lab cover sheet on top of all the materials you are submitting.
- Submit your work in the ***order*** listed above.
- Your lab packet is due by 9 AM on the day after the lab is performed. You may do your (late) demonstration after submitting your lab packet if necessary. There is a 1 point per day late penalty on the demo. The maximum late penalty for the report+demo per day is 2 points. Slip your submitted lab packet under my office door or submit your packet to me during the laboratory.