MSOE EECS Department
CE-1901: Week 8 Lab Grading Checklist
Dr. Yoder Name:

Item	Points
Prelab 2 VHDL : RCA4 structural VHDL, RTL, simulation	/ 6
Prelab 2 RCA4 laboratory board demo	/ 2
In-class 2: VHDL: RCA8 structural VHDL – allowing RCA4 rippled to RCA4 **or** FA rippled 8 times , RTL, simulation	/ 5
In-class 3: VHDL: RCA32 structural VHDL – allowing RCA8 rippled 4 times, RCA4 rippled 8 times, FA rippled 32 times, RTL, simulation	/ 5
Following Submission Instructions	/ 2
Total	/ 20

- ***Staple*** this lab cover sheet on top of all the materials you are submitting.
- Submit design work, VHDL code, RTL, and simulation waveforms for each problem.
- Submit your work in the ***order*** listed above.
- Your lab packet is due by 9 AM on the day after the lab is performed. You may do your (late) demonstration after submitting your lab packet if necessary. There is a 1 point per day late penalty on the demo. The maximum late penalty for the report+demo per day is 2 points. Slip your submitted lab packet under my office door or submit your packet to me during the laboratory.