MSOE EECS Department
CE-1901: Week 9 Lab Grading Checklist
Dr. Yoder Name:

Item	Points
Prelab 2: Full adder ("full adder" always means "1-bit"): VHDL	/ 3
Prelab 2: CLC4 behavioral VHDL, RTL. (Simulation optional)	/ 3
Prelab 2: CLA4 structural VHDL, RTL, simulation	/ 3
Prelab 2: CLC4 laboratory board demo	/ 3
In-lab 2: VHDL: Carry-Select adder: VHDL and RTL for all new VHDL files. Simulation of overall circuit	/ 6
Following Submission Instructions	/ 2
Total	/ 20

- ***Staple*** this lab cover sheet on top of all the materials you are submitting.
- Submit design work, VHDL code, RTL, and simulation waveforms for each problem.
- Submit your work in the ***order*** listed above.
- Your lab packet is due by 9 AM on the day after the lab is performed. You may do your (late) demonstration after submitting your lab packet if necessary. There is a 1 point per day late penalty on the demo. The maximum late penalty for the report+demo per day is 2 points. Slip your submitted lab packet under my office door or submit your packet to me during the laboratory.