

VHDL Lab Checklist

Name: _____

CE1911

Lab: _____

VHDL Design Process

	Yes	No
Includes a block comment at the top of the file with <ul style="list-style-type: none"> Your name The class number The lab number The date A brief description of what the file is about Includes the IEEE libraries and packages after the block comment		
Names entity and architecture appropriately (no joking with the architecture name!). Names signals appropriately.		
Indents everything between the architecture and the begin statement. Aligns the architecture with the begin statement. Indents all multi-line structures (e.g. process, if, when-else)		
Declares internal signals to hold the finite state machine state		
Uses hand encoding or abstract state types appropriately		
Includes comments to delineate the state register, next state logic, and output logic		
Implements state machines using clear and correct VHDL syntax		
Demonstrates mature use of with-select, when-else, and process syntax		
Completes with-select with when others clause. Completes when-else with else X;		
Monitors printed design files for line wraps that make code hard to read. Controls lines with breaks around 50 or 60 characters. Inserts line breaks where needed to keep code readable		

Design, Simulation, and Test

Examines RTL diagrams during the design process		
Prints RTL to verify an FSM was created		
Creates a simulation for the system		
Includes appropriate waveforms in simulation. Puts inputs above outputs		
Adds reset signal to force FSM into a known starting state		
Clocks sufficient times to ensure simulation provides value		
Implements input waveforms to stimulate the FSM to transition state		
Annotates simulation (and Waveforms if req.) output to verify results		
Demonstrates working circuit in the laboratory environment		

Report

Staples this sheet as a cover. Puts remaining sheets in order : any paper design, VHDL, RTL, simulation.		
Total (out of 20)		

Your demo is due during the lab period. Your lab packet is due by 10 AM on the day after the lab is performed. You may do your (late) demonstration after submitting your lab packet if necessary. There is a 1 point per day late penalty on the demo.

The maximum late penalty for the report+demo per day is 2 points. Submit your packet to me during the laboratory or slip it under my office door.

Complete example VHDL Moore Machine

```
-- Josiah Yoder
-- CE1901
-- Lab 4 (In-class prep)
-- 18 Mar 2016
-- Simulates a snail that smiles when it reads 1 0 in sequence from a.
library ieee;
use ieee.std_logic_1164.all;

entity snail is
    port(
        a: in std_logic; -- will read one value at a time from here
        clock: in std_logic;
        rstn: in std_logic; -- asynch reset
        y: out std_logic -- 1 for smiling
    );
end entity;

architecture internals of snail is
    type statetype is (nothing, have1, have10);
    signal state: statetype;
    signal nextstate: statetype;
begin

    -- state register
    process(clock,rstn)
    begin
        if rstn = '0'
        then
            state <= nothing;
        elsif rising_edge(clock)
        then
            state <= nextstate;
        end if;
    end process;

    -- next state logic
    nextstate <=
        have1 when (a='1') else
        nothing when (a='0' and (state=nothing or state=have10)) else
        have10; -- when (a='0' and state=have1)

    -- output logic
    y <=
        '1' when state=have10 else
        '0';

end architecture;
```